

# MUSIC SYNTHESIZER SY99

## SERVICE MANUAL



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## IMPORTANT NOTICE

This manual has been provided for the use of authorized Yamaha Retailers and their service personnel. It has been assumed that basic service procedures inherent to the industry, and more specifically Yamaha Products, are already known and understood by the users, and have therefore not been restated.

**WARNING:** Failure to follow appropriate service and safety procedures when servicing this product may result in personal injury, destruction of expensive components and failure of the product to perform as specified. For these reasons, we advise all Yamaha product owners that all service required should be performed by an authorized Yamaha Retailer or the appointed service representative.

**IMPORTANT:** The presentation or sale of this manual to any individual or firm does not constitute authorization, certification, recognition of any applicable technical capabilities, or establish a principle-agent relationship of any form.

The data provided is believed to be accurate and applicable to the unit(s) indicated on the cover. The research, engineering, and service departments of Yamaha are continually striving to improve Yamaha products. Modifications are, therefore, inevitable and changes in specification are subject to change without notice or obligation to retrofit. Should any discrepancy appear to exist, please contact the distributor's Service Division.

**WARNING:** Static discharges can destroy expensive components. Discharge any static electricity your body may have accumulated by grounding yourself to the ground buss in the unit (heavy gauge black wires connect to this buss).

**IMPORTANT:** Turn the unit OFF during disassembly and parts replacement. Recheck all work before you apply power to the unit.

This product uses a lithium battery for memory back-up.

**WARNING:** Lithium batteries are dangerous because they can be exploded by improper handling. Observe the following precautions when handling or replacing lithium batteries.

- Leave lithium battery replacement to qualified service personnel.
- Always replace with batteries of the same type.
- When installing on the PC board, solder using the connection terminals provided on the battery cells. Never solder directly to the cells. Perform the soldering as quickly as possible.
- Never reverse the battery polarities when installing.
- Do not short the batteries.
- Do not attempt to recharge these batteries.
- Do not disassemble the batteries.
- Never heat batteries or throw them into fire.

### ADVARSEL!

Lithiumbatteri. Eksplosionsfare.

Udskiftning må kun foretages af en sagkyndig, og som beskrevet i servicemanualen.

## WARNING: CHEMICAL CONTENT NOTICE!

The solder used in the production of this product contains LEAD. In addition, other electrical/electronic and/or plastic (where applicable) components may also contain traces of chemicals found by the California Health and Welfare Agency (and possibly other entities) to cause cancer and/or birth defects or other reproductive harm.

**DO NOT PLACE SOLDER, ELECTRICAL/ELECTRONIC OR PLASTIC COMPONENTS IN YOUR MOUTH FOR ANY REASON WHAT SO EVER!**

Avoid prolonged, unprotected contact between solder and your skin! When soldering, do not inhale solder fumes or expose eyes to solder/flux vapor!

If you come in contact with solder or components located inside the enclosure of this product, wash your hands before handling food.

## ■ SPECIFICATIONS (総合仕様)

### Tone generator: Realtime Convolution and Modulation (RCM)

AWM2: 16 bit linear waveform data, maximum 48 kHz sampling frequency

AFM: 6 operators, 45 algorithms, 3 feedback loops, 16 waveforms, modulation from AWM output

Filter: Time variant IIR (infinite impulse response) digital filters, 2 filters for each element (maximum of 8 filters per voice)

Maximum simultaneous notes: 16 (Voice mode), 32 (Multi mode)

Maximum simultaneous timbres: 1 (Voice mode), 16 (Multi mode)

Note assignment: Last note priority, DVA (dynamic voice allocation)

**Keyboard:** 76 notes, key velocity sensitivity, channel aftertouch (with zoned aftertouch)

**DSP effects:** 2 units, 63 effect types

### Sequencer:

Tracks: 16 (15 tracks + 1 pattern track)

Songs: 10

Resolution: 1/96 of a quarter note (for internal clock), 1/24 of a quarter note (for MIDI sync)

Maximum simultaneous notes: 32

Capacity: approximately 27,000 notes

Patterns: 99

Recording: realtime/step/punch in

### Memory:

Preset memory: 128 voices, 16 multis

Internal memory: 64 voices, 16 multis

Waveform memory: 4 Mwords (8 Mbytes), 267 sounds

MDR/sample memory: 512 kbytes (expandable to 1.5 Mwords)

Card slots: synthesizer data × 1, waveform data × 1

Disk: 3.5" floppy disk drive (720 kbyte formatted)


### Controllers:

Wheels: PITCH, MODULATION 1, MODULATION 2

Slider: OUTPUT 1, OUTPUT 2, DATA ENTRY

Knobs: LCD contrast, click volume

Dial: data entry dial

Panel switches: MODE × 5, EDIT/COMPARE, COPY/SAVE, EF.BYPASS, SEQUENCER × 7, SHIFT, function × 8, EXIT, PAGE < >, JUMP/MARK, cursor Δ ▽ < >, -1/NO, +1/YES, numeric keypad 0-9, ENTER, , MEMORY × 4, BANK × 4, voice select × 16,

### Display:

LCD: 240 × 64 pixels (with backlight)

LED: red × 11, red/green × 21

### Terminals:

Audio output: OUTPUT 1 (L/MONO, R), OUTPUT 2 (L, R), PHONES

Controller: BREATH, FOOT VOLUME, FOOT CONTROLLER, SUSTAIN, FOOT SWITCH

MIDI: IN, OUT, THRU

### Power requirements:

UL, CSA: 120V

Europe, WG, Australia, BS: 220-240V

### Power consumption:

UL, CSA: 35W

Europe, WG, Australia, BS: 35W

### Dimensions:

1254(W) × 407(D) × 120(H) mm

### Weight: 19.6 kg

### Output level:

Headphones: +5.5dBm (150Ω load)

Outputs: 0dBm (10kΩ load)

## &lt;機能&gt;

## 音源:

## 音源形式:

- RCM音源
- AWM2: 16ビットリニア波形, サンプル周波数 f 24/32/48kHz
- 1音(エレメント)につき1オクターブ12dBのデジタルフィルターを2個搭載
- 内蔵波形容量
- ROM部: 4メガワード(8MByte)
- RAM部: 256キロワード(512KByte) バッテリーバックアップ拡張スロットに増設メモリーボードを差すことにより、最大1.5メガワード(3MByte)まで拡張可能
- AFM: 6オペレータ、45アルゴリズム、3系統フィードバック、16波形
- AWM2の出力波形による変調が可能
- 1音(エレメント)につき1オクターブ12dBのデジタルフィルターを2個搭載

## フィルター:

- 時変形デジタルフィルター×最大8/ボイス
- 各フィルターはLPF, HPFの切り替えができ、この組み合わせによりBPFやローパス24dBのLPFとしても使用可能
- レゾナンス可変で共振領域までカバー

## 最大同時発音数:

- AWM2: 16音+AFM: 16音

## 最大同時音色数:

- 16

## 発音形式:

- 後着優先、DVA

## 鍵盤:

- 76キー/イニシャル&チャンネルアフータッチ付き

## エフェクタータイプ:

- 高品位DSPを2基搭載(シリアルまたはパラレル接続)
- プログラム数63
- エフェクトパラメーターをリアルタイムにコントロール可(2系統)

## シーケンサー:

## トラック数:

- 16トラック(含むパターントラック1)

## ソング:

- 10 (Next Song, Next Mode付)

## 分解能:

- 1/96 (内部クロック時)

## 最大同時発音数:

- 32

## 最大記憶音数:

- 約27000音

## パターン数:

- 99

## 録音方式:

- リアルタイム/ステップ/パンチイン

## &lt;内部構成&gt;

## プリセットメモリー:

- ボイス: 128+マルチ: 16

## インターナルメモリー:

- ボイス: 64+マルチ: 16

## 波形用メモリー:

- ROM: 4メガワード(8MByte)
- PRESET 1=155, PRESET 2=112
- RAM: 512 KByte (RAM ボードの追加により最大3072 KByteまで拡張可)
- MIDIサンプルダンプ、ディスク、ウェイブフォームカードより供給

## カードスロット:

- 音色パラメータ用×1
- MCD64: 1バンク
- ※1バンク: 64ボイス+16マルチ 1システム
- 波形用×1

## 3.5インチFDD:

- 1 (フォーマット時713KB)

## &lt;操作子&gt;

## Wheel:

- ピッチベンド、モジュレーション1、モジュレーション2

## スライダーボリューム:

- アウトプットボリューム1・2、データエントリー

## ロータリーボリューム:

- LCD コントロール、クリックボリューム

## ダイヤル:

- データエントリー

## パネルスイッチ:

- Mode(5)Voice, Multi, Song, Pattern, Utility
- Edit(2)Edit/Compare, Copy
- Effect bypass(1)
- Memory select(4)Preset 1, Preset 2, Internal, Card
- Bank select (4)A ~ D
- Program select(1)1 ~ 16
- Page(3)Page+, Page-, Jump/Mark
- テンキー(12)0 ~ 9, Enter, -
- Data Entry(2)Inc, Dec
- カーソル(4)←, →, ↑, ↓
- Function(8)function 1 ~ 8, Shift, Exit
- Sequencer(7)Run, Stop, Rec, Top, Rew, FF, Auto Locate

## &lt;ディスプレイ&gt;

## LCD:

- 240×64 Dots(バックライト付き)

## LED:

- Red×11
- Red/Green×21

## &lt;接続端子&gt;

## 音声出力:

- 4 Output1(L/Mix L/Mono, R/Mix R), Output2(L,R)

## ヘッドフォン:

- 1

## コントローラ:

- 5 Foot control, Foot volume, Foot switch, Sustain switch, Breath control

## MIDI:

- 3 IN, OUT, THRU

## &lt;出力レベル&gt;

## ヘッドフォン:

- +5.5dBm (150Ω)

## リア出力端子:

- 0 dBm (10kΩ)

## &lt;電源(国内)&gt;

## 電源電圧:

- 100V

## 消費電力:

- 25W

## &lt;寸法、重量&gt;

## 寸法:

- 1254(W)×407(D)×120(H)(mm)

## 重量:

- 19.6kg

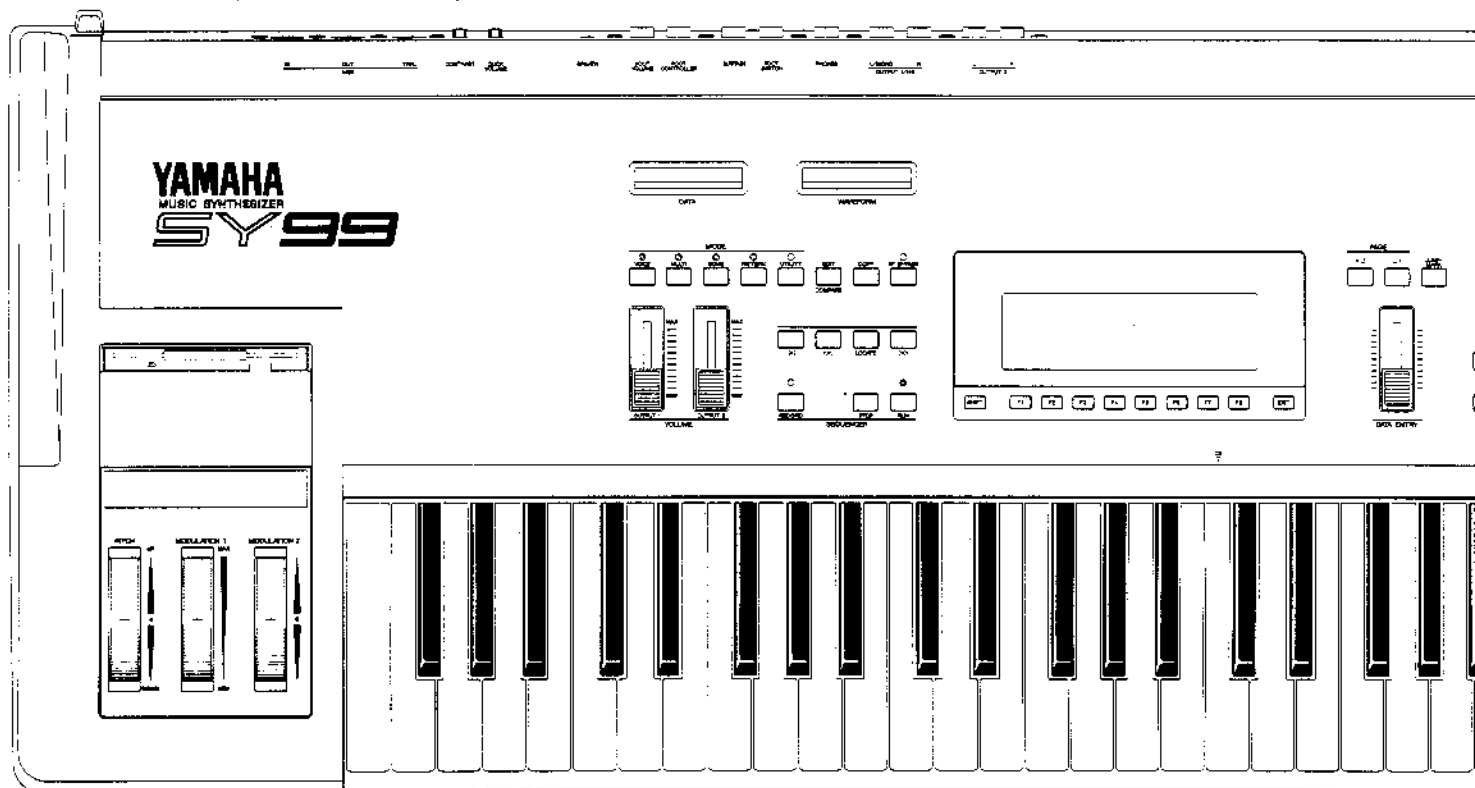
## &lt;付属品&gt;

- デモディスク2枚(3.5インチフロッピーディスク)



## ■PANEL LAYOUT (パネルレイアウト)

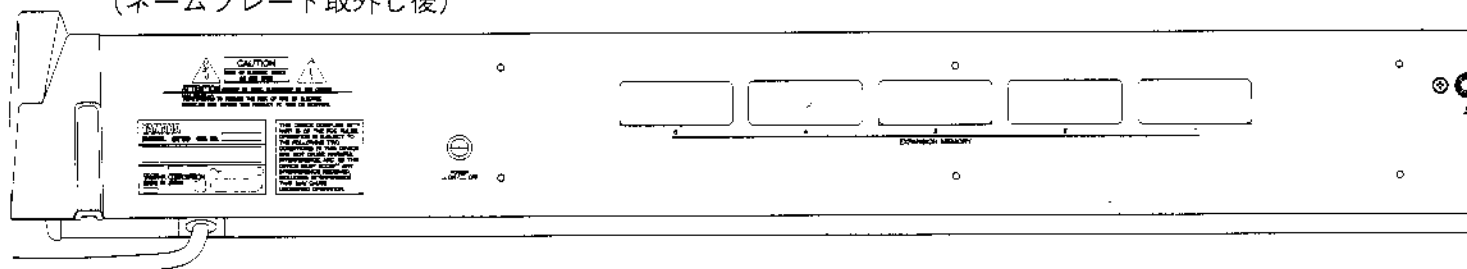
● **Front Panel** (フロントパネル)

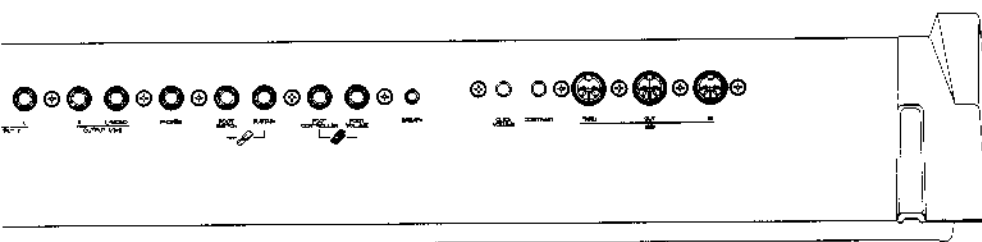
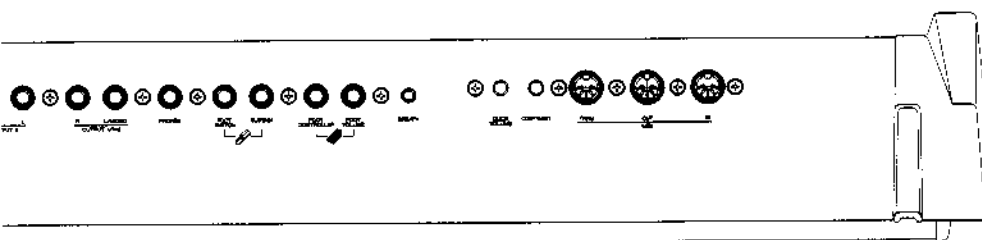
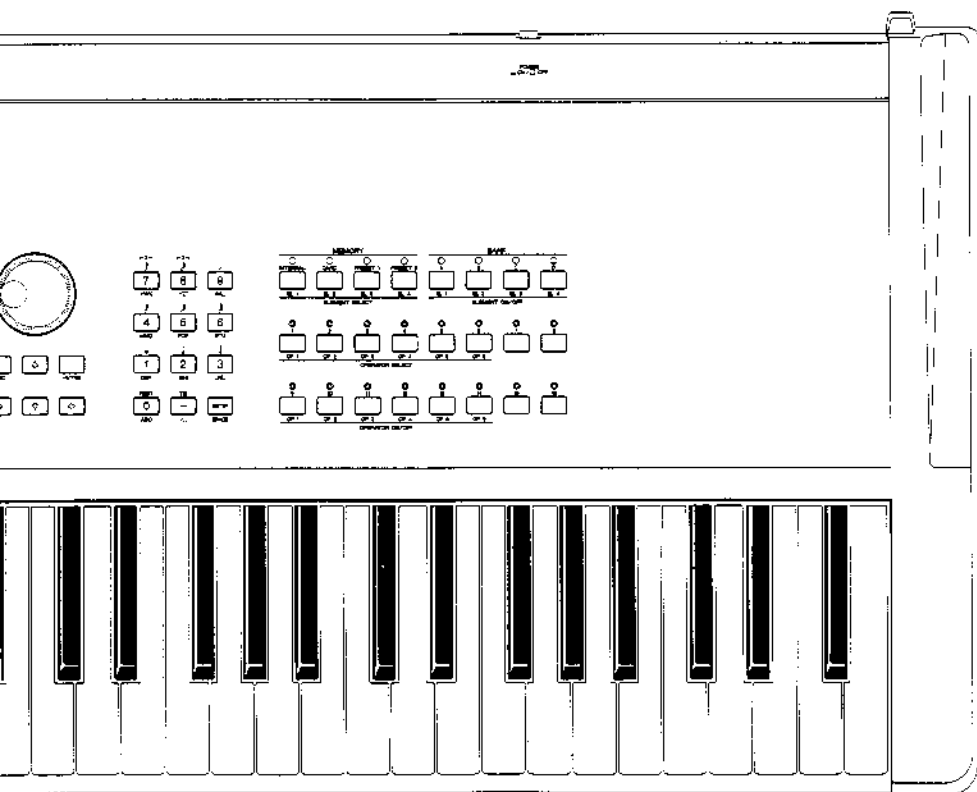


● Rear Panel (リアパネル)

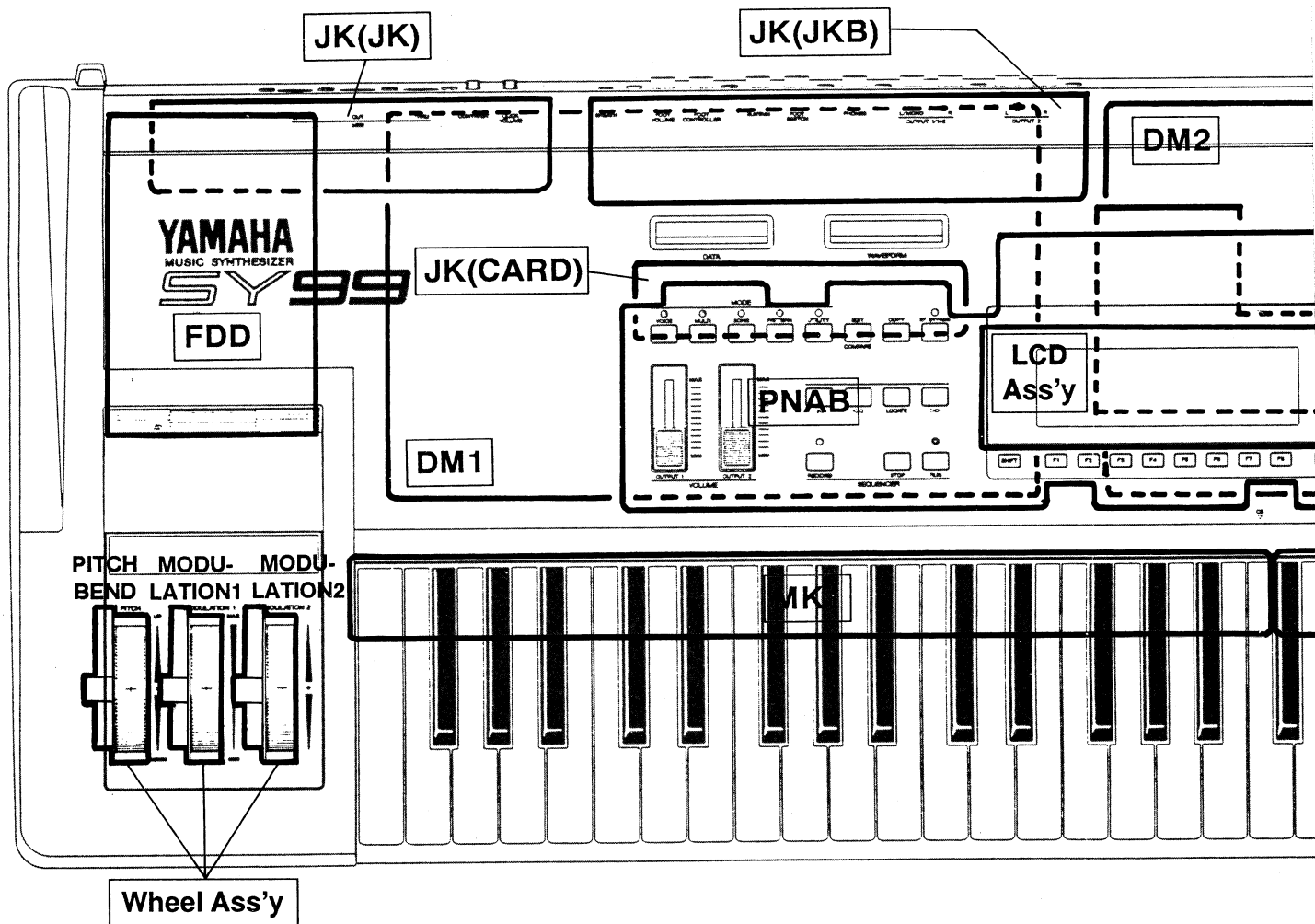


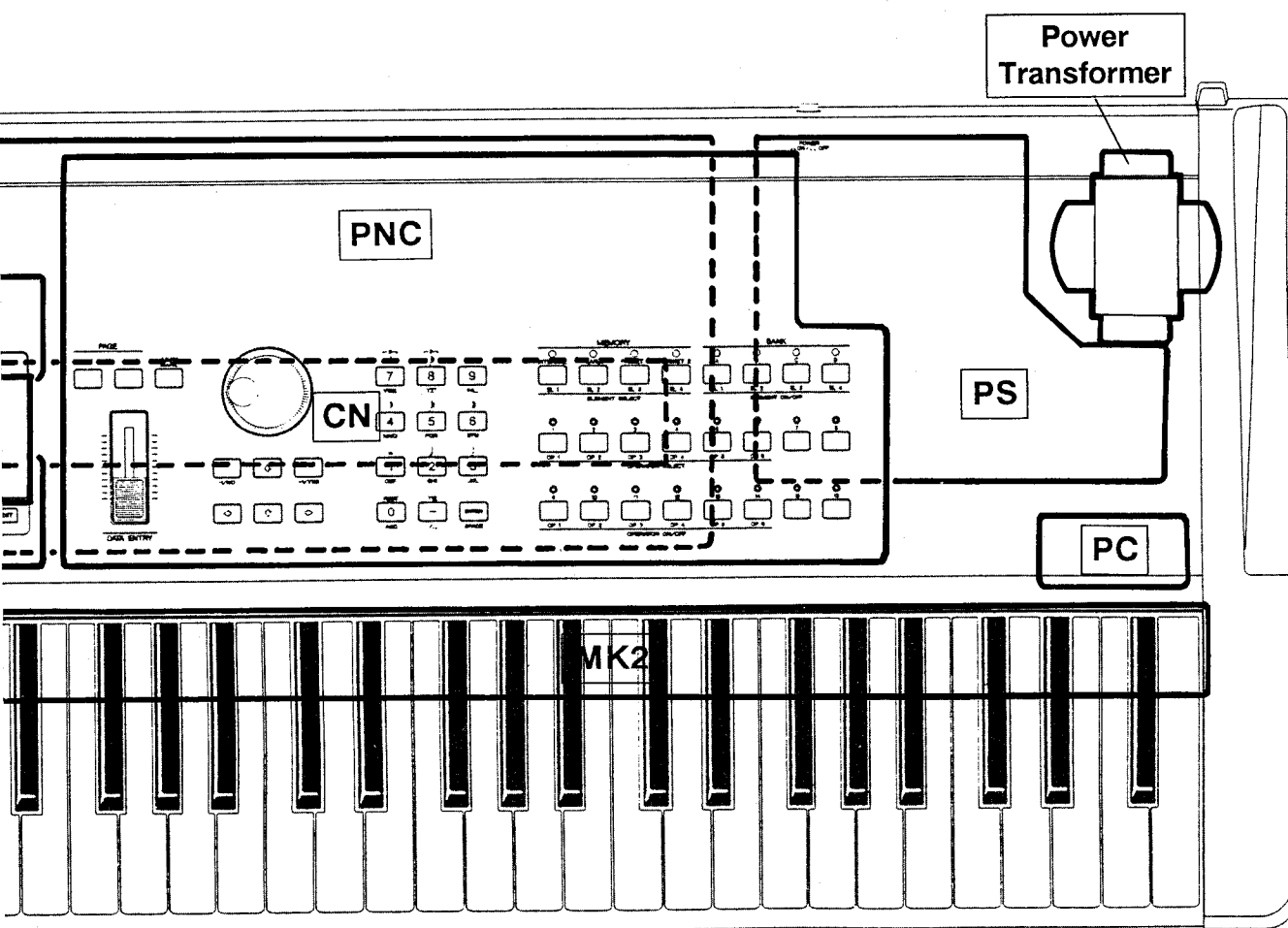
After the name plate has been removed ;  
(ネームプレート取外し後)



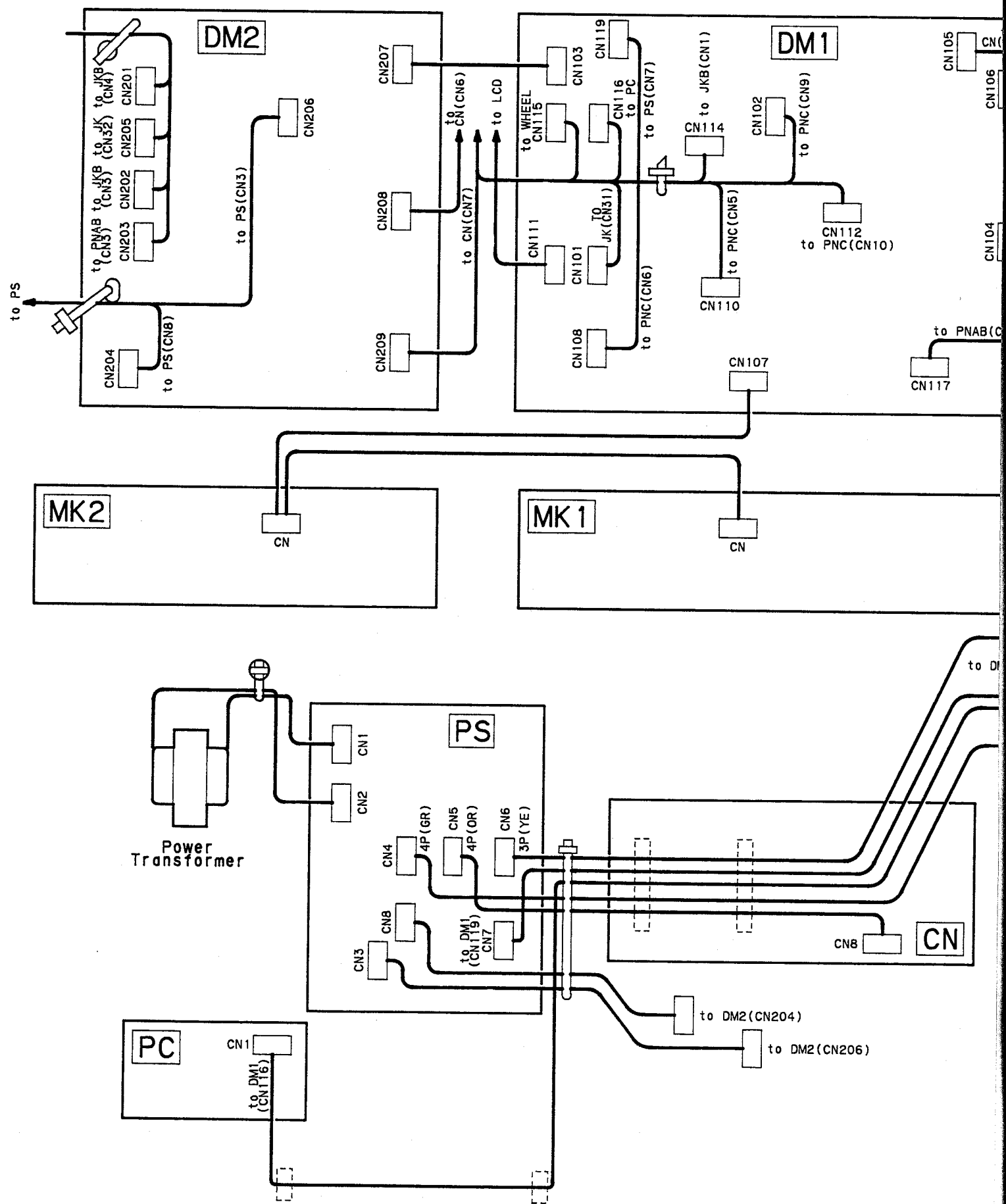


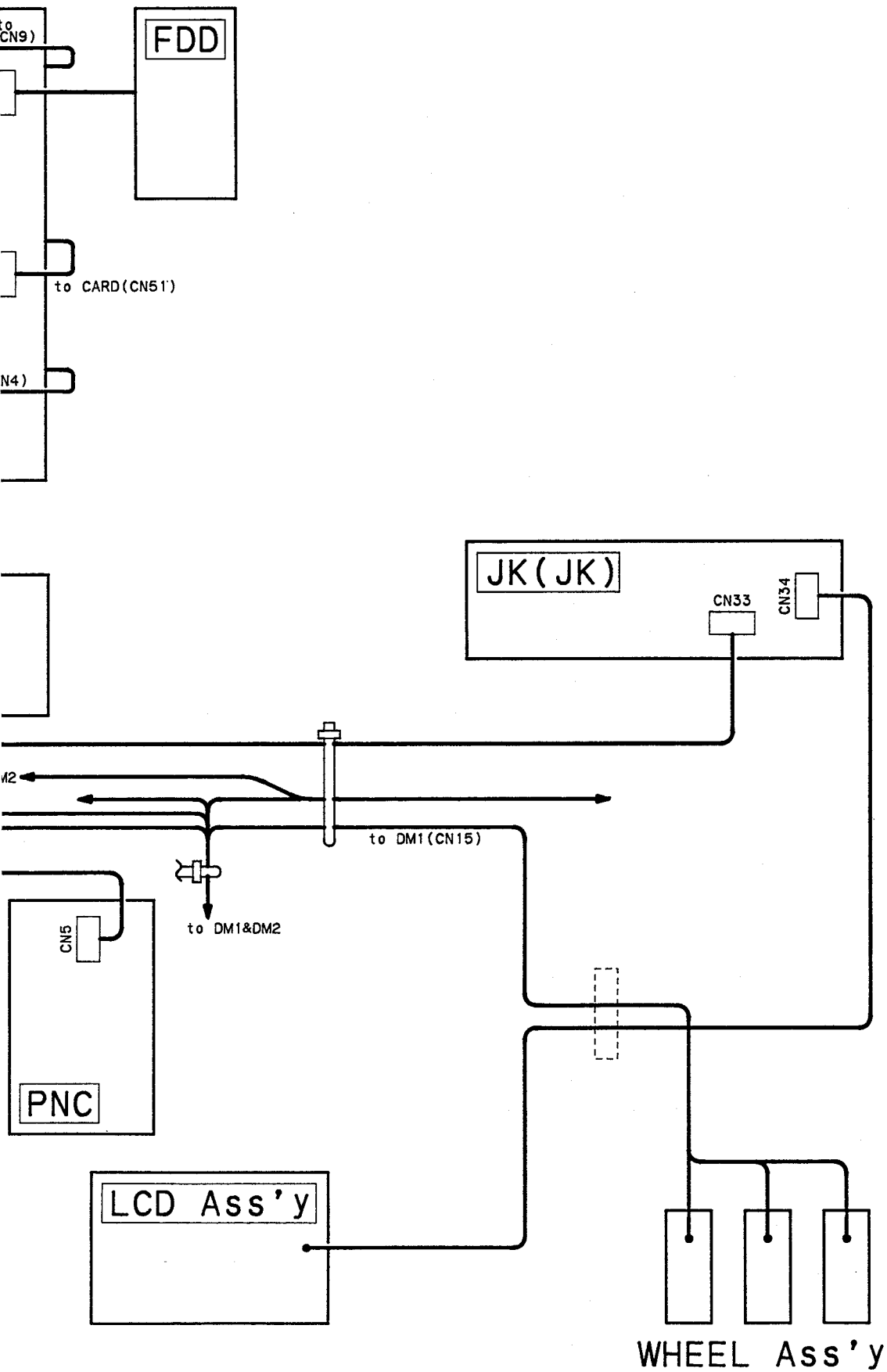
# **■CIRCUIT BOARD LAYOUT (ユニットレイアウト)**

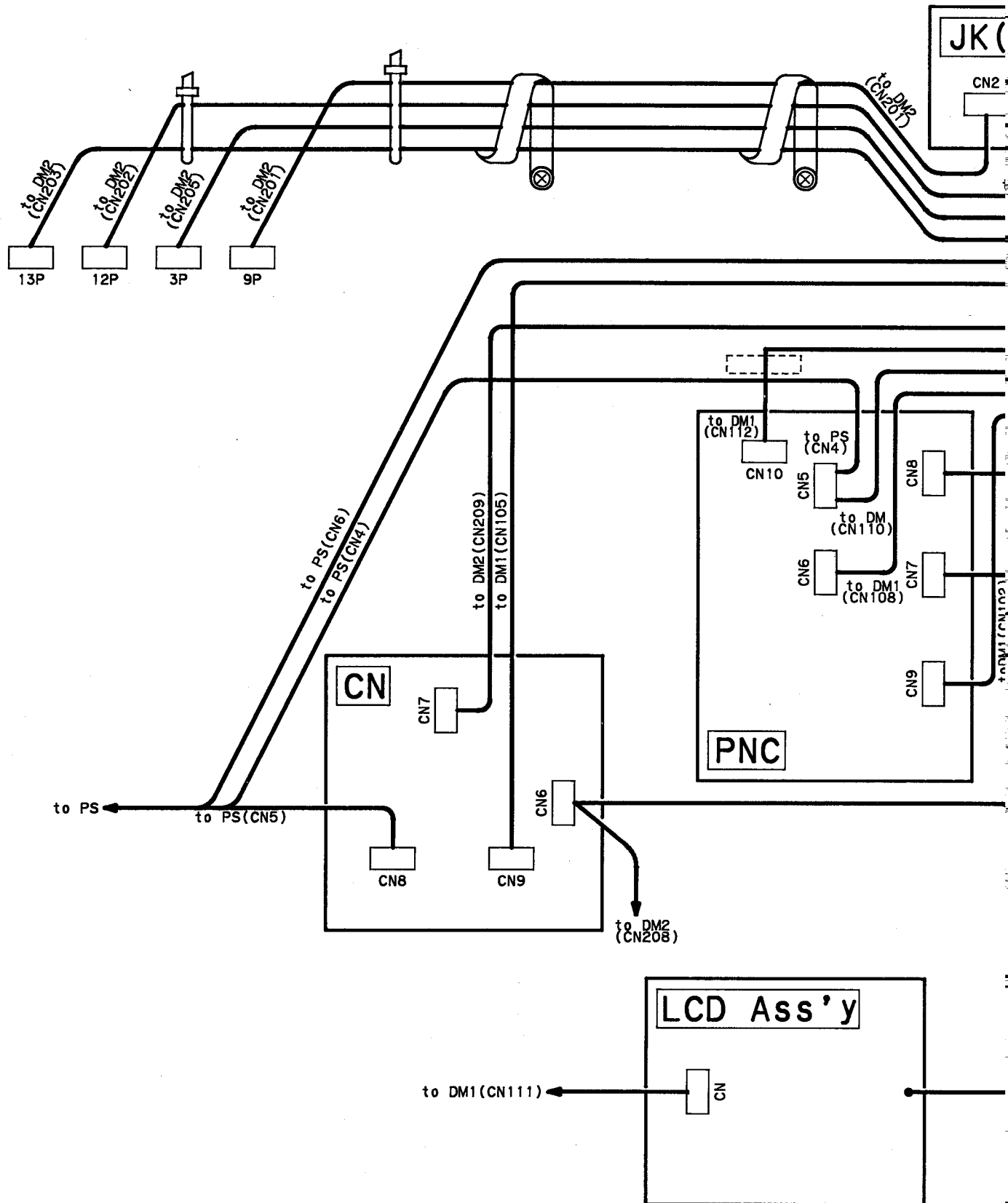


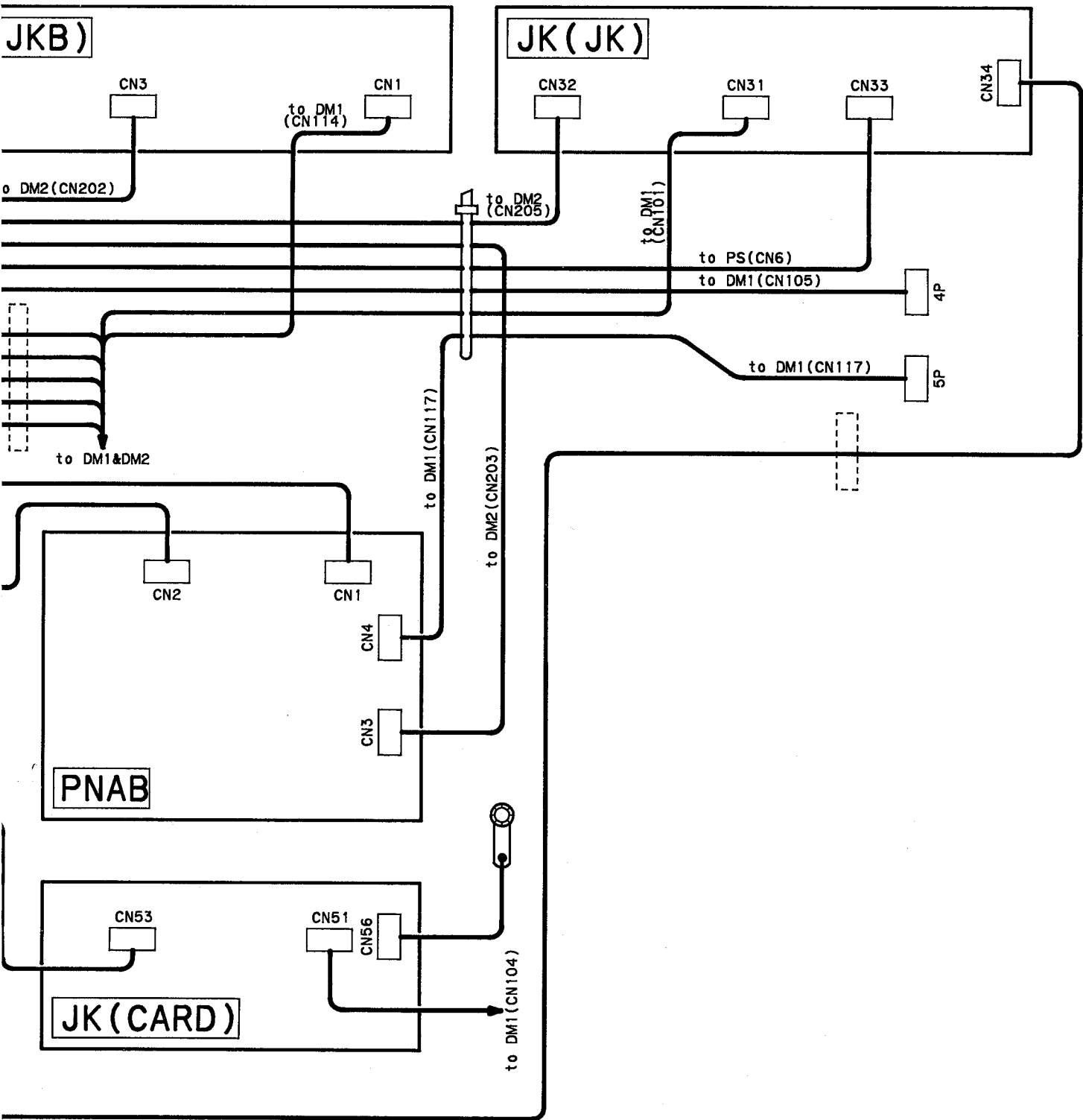


■ WIRING (結線図)



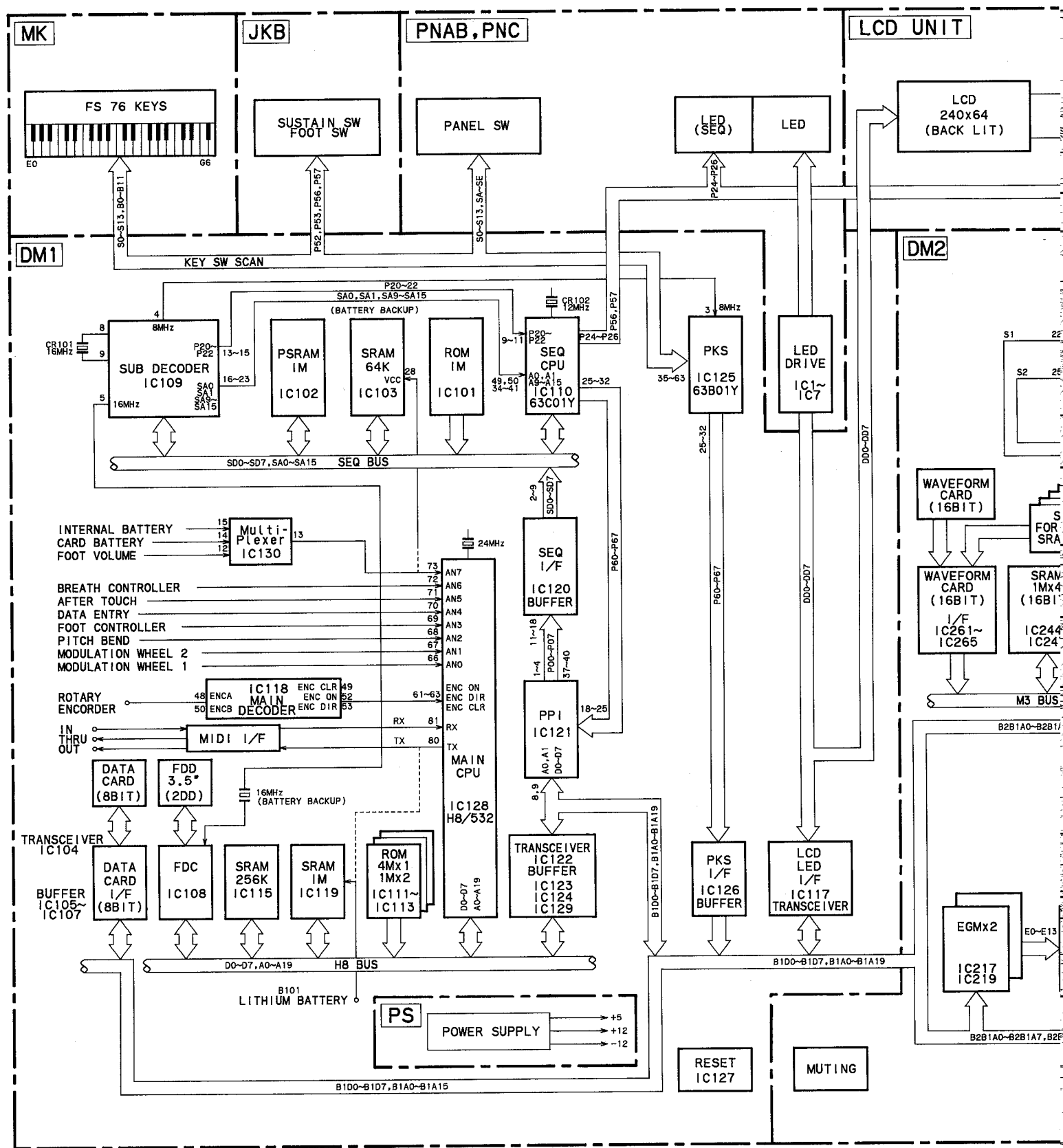


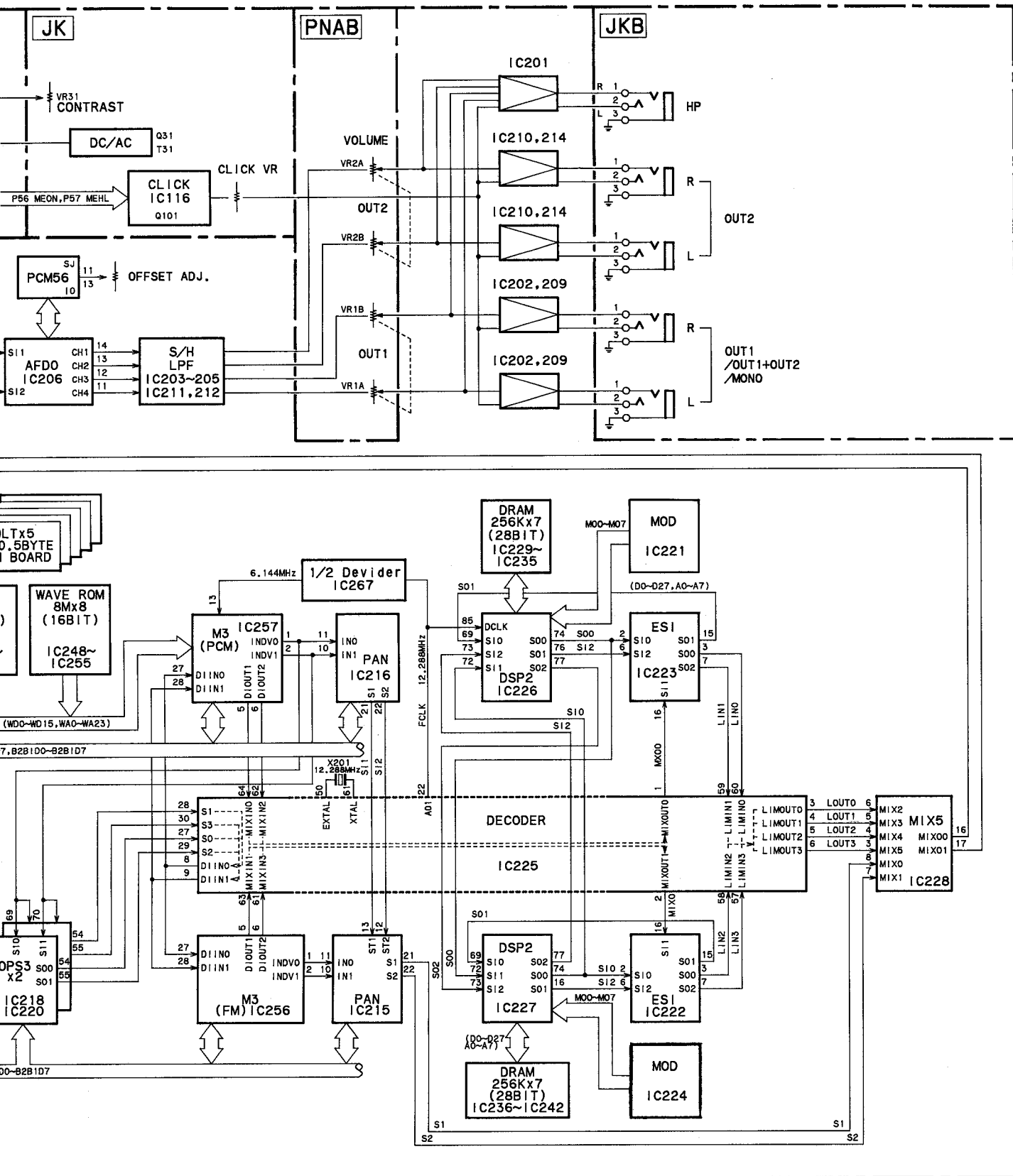






# BLOCK DIAGRAM (ブロックダイアグラム)





## ■ DISASSEMBLY PROCEDURE (分解手順)

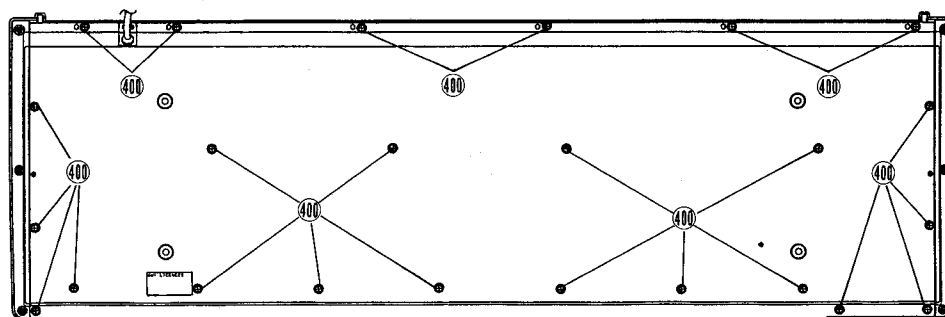
### 1. Bottom Cover Assembly Removal

- 1-1. Remove the twenty-four (24) screws marked ④①①, the bottom cover assembly can be removed. (Fig. 1)

\* This will give you access to the DM1, DM2, PS circuit boards, FDD assembly and wheel assembly.

### 1. 底板Ass'yの外し方

- 1-1. ④①① のネジ24本を外して底板Ass'yを取り外します。  
(図 1)



④①① : 4.0 x 8 Bonding Tapping Screw (ボンディングタッピングネジ)

(Fig. 1)

### 2. DM1 Circuit Board Removal

- 2-1. Remove the bottom cover assembly. (see procedure 1)  
2-2. Remove the six (6) screws marked ③⑧①, the DM1 circuit board can be raised. (Fig. 2)  
After the connectors have been disconnected, the DM1 circuit board can be taken out of the unit completely.

### 2. DMIシートの外し方

- 2-1. 底板Ass'yを外します。(1項参照)  
2-2. ③⑧① のネジ6本を外しコネクタを抜いて、DMIシートを取り外します。(図 2)

### 3. DM2 Circuit Board Removal

- 3-1. Remove the bottom cover assembly. (see procedure 1)  
3-2. Remove the six (6) screws marked ③⑧①, the DM2 circuit board can be raised. (Fig. 2)  
After the connectors have been disconnected, the DM2 circuit board can be taken out of the unit completely.

### 3. DM2シートの外し方

- 3-1. 底板Ass'yを外します。(1項参照)  
3-2. ③⑧① のネジ6本を外しコネクタを抜いて、DM2シートを取り外します。(図 2)

### 4. Power Supply Assembly Removal

- 4-1. Remove the bottom cover assembly. (see procedure 1)  
4-2. Remove the screw marked ④①① to remove the AC panel. (Fig. 2)  
4-3. The power supply assembly can be removed by removing the four (4) screws marked ②⑤① and disconnecting the connectors. (Fig. 2)

### 4. 電源Ass'yの外し方

- 4-1. 底板Ass'yを外します。(1項参照)  
4-2. ④①① のネジ1本を外し、ACパネルを外しておきます。  
(図 2)  
4-3. ②⑤① のネジ4本を外しコネクタを抜いて、電源Ass'yを取り外します。(図 2)

## 5. Power Transformer Removal

- 5-1. Remove the bottom cover assembly. (see procedure 1)
- 5-2. Remove the two (2) screws marked ②③① and disconnect the connectors, then remove the power transformer. (Fig. 2)

## 6. FDD Assembly Removal

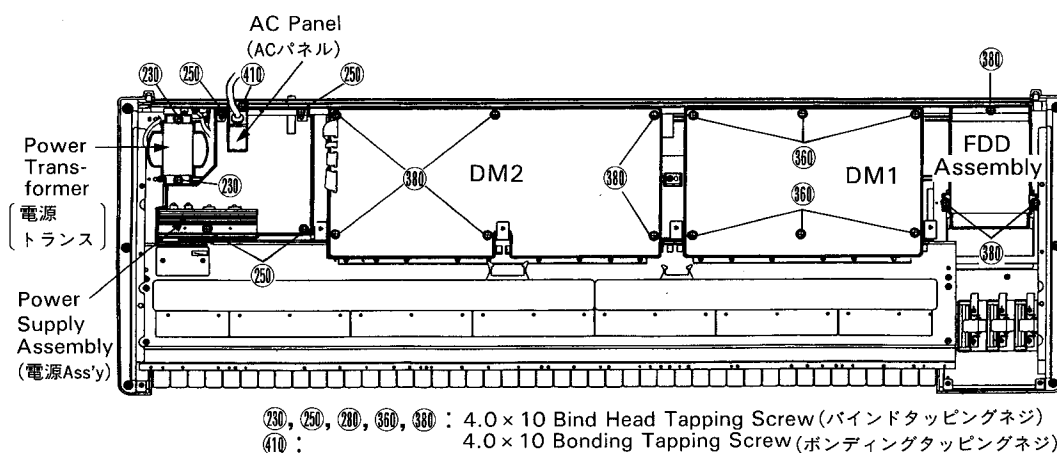
- 6-1. Remove the bottom cover assembly. (see procedure 1)
- 6-2. Remove the three (3) screws marked ②③① and disconnect the connectors, the FDD assembly can be taken out of the SY99 unit. (Fig. 2)
- 6-3. To remove the FDD bracket from the FDD assembly, remove the four (4) screws marked ③①. (Fig. 3)

## 5. 電源トランスの外し方

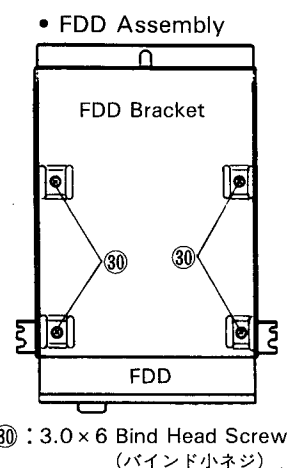
- 5-1. 底板Ass'yを外します。(1項参照)
- 5-2. ②③①のネジ2本を外しコネクターを抜いて、電源トランスを取り外します。(図 2)

## 6. FDD Ass'y の外し方

- 6-1. 底板Ass'yを外します。(1項参照)
- 6-2. ②③①のネジ3本を外しコネクターを抜いて、FDD Ass'yを取り外します。(図 2)
- 6-3. FDD金具は、③①のネジ4本を外して取り外します。(図 3)



(Fig. 2)



(Fig. 3)

## 7. Keyboard Assembly Removal

- 7-1. Remove the bottom cover assembly. (see procedure 1)
- 7-2. Remove the DM1 and DM2 circuit boards. (see procedures 2 and 3)
- 7-3. Remove the isolation sheet located under the DM2 circuit board.
- 7-4. The keyboard assembly can be removed by removing the four (4) screws marked ④⑤, four (4) screws marked ④⑥, eight (8) screws marked ④⑦ and six (6) screws marked ④⑧. (Fig. 4)

## 8. JK (JK, JKB, CARD) circuit boards Removal

- 8-1. Remove the bottom cover assembly. (see procedure 1)
- 8-2. Remove the DM1 circuit board. (see procedure 2)
- 8-3. Raise the DM1 shield sheet up to this side. (Fig. 4)

## 7. 鍵盤Ass'yの外し方

- 7-1. 底板Ass'yを外します。(1項参照)
- 7-2. DM1シートとDM2シートを外します。(2、3項参照)
- 7-3. DM2シートの下側にある、絶縁シートを外します。
- 7-4. ④⑤のネジ4本と④⑥のネジ4本、④⑦のネジ8本、④⑧のネジ6本を外し、MKシートのコネクターを抜いて、鍵盤Ass'yを取り外します。(図 4)

## 8. JK(JK,JKB,CARD)シートの外し方

- 8-1. 底板Ass'yを外します。(1項参照)
- 8-2. DM1シートを外します。(2項参照)
- 8-3. DM1シールドシートを手前に起こします。(図 4)

#### 8-4. JK (JK) circuit board removal

8-4-1. Remove the FDD assembly. (see procedure 6)

8-4-2. Remove the four (4) screws marked (290a) and one (1) screw marked (295) on the rear panel and disconnect the connector, the JK (JK) circuit board can be removed. (Fig. 5 and Fig. 6)

#### 8-5. JK (JKB) circuit board removal

8-5-1. Remove the six (6) screws marked (290b) on the rear panel, the JK (JKB) circuit board can be removed. (Fig. 5 and Fig. 6)

#### 8-6. JK (CARD) circuit board removal

8-6-1. There are four (4) screws marked (270), three (3) on the CARD circuit board and one on the lug terminal. After these screws have been removed, the JK (CARD) circuit board can be removed. (Fig. 5)

#### 8-4. JK(JK)シートの外し方

8-4-1. FDD Ass'yを外します。(6項参照)

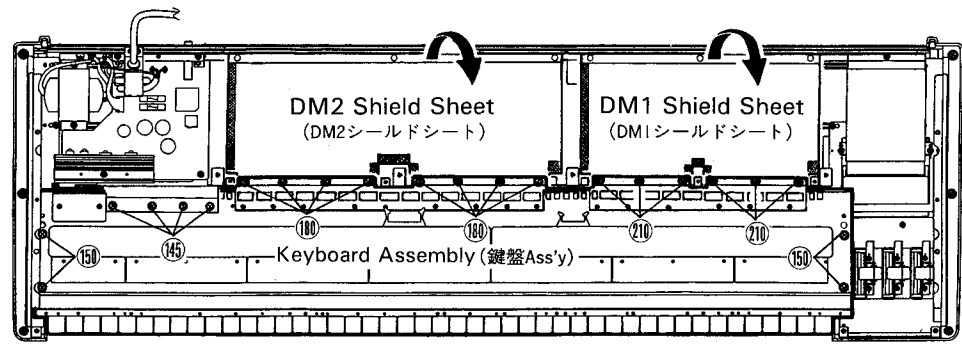
8-4-2. リア側よりJK(JK)シートを止めている(290a)のネジ4本と(295)のネジ1本を外し、コネクターを抜いて、JK(JK)シートを取り外します。(図 5、6)

#### 8-5. JK(JKB)シートの外し方

8-5-1. リア側よりJK(JKB)シートを止めている(290b)のネジ6本を外して、JK(JKB)シートを取り外します。(図 5、6)

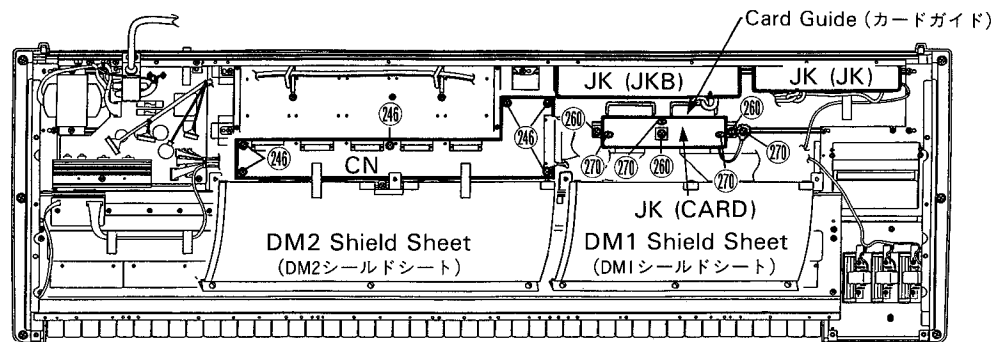
#### 8-6. JK(CARD)シートの外し方

8-6-1. (270)のネジ4本(CARDシート:3本、ラグ端子:1本)を外し、コネクターを抜いて、JK(CARD)シートを取り外します。(図 5)



(145) : 3.0×6 Bind Head Screw (バインド小ネジ) (150) : 4.0×16 Bind Head Tapping Screw (バインドタッピングネジ)  
(180, 210) : 4.0×10 Bind Head Tapping Screw (バインドタッピングネジ)

(Fig. 4)

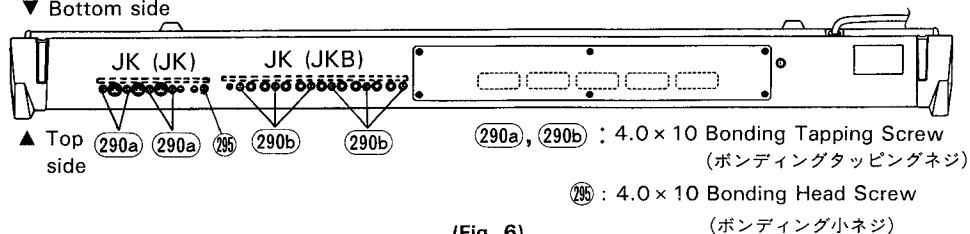


(246) : 3.0×6 Bind Head Screw (バインド小ネジ) (260, 270) : 4.0×10 Bind Head Tapping Screw (バインドタッピングネジ)

(Fig. 5)

#### • Rear view

##### ▼ Bottom side



(Fig. 6)

## 9. CN Circuit Board Removal

- 9-1. Remove the bottom cover assembly. (see procedure 1)
- 9-2. Remove the DM1 and DM2 circuit boards. (see procedures 2 and 3)
- 9-3. Remove the isolation sheet located under the DM2 circuit board.
- 9-4. Raise the DM1 and DM2 shield sheets up to this side. (Fig. 4)
- 9-5. Remove the six (6) screws marked ②⑤ and disconnect the connector, then remove the CN circuit board. (Fig. 5)

## 10. Slot Unit Removal

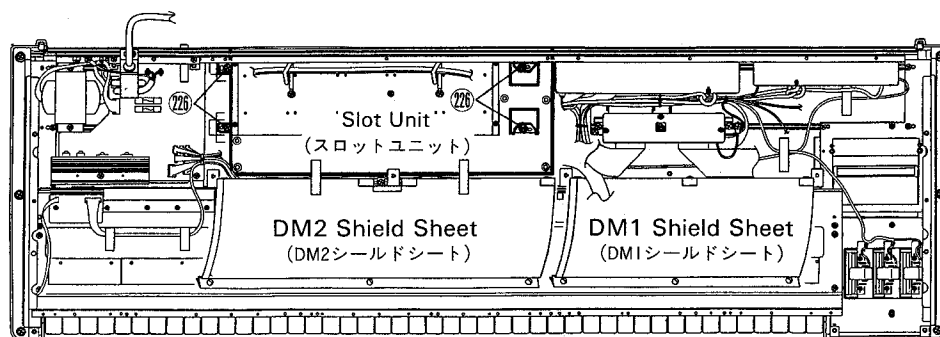
- 10-1. Remove the bottom cover assembly. (see procedure 1)
- 10-2. Remove the DM1 and DM2 circuit boards. (see procedures 2 and 3)
- 10-3. Remove the CN circuit board. (see procedure 9)
- 10-4. To remove the slot unit, remove the four (4) screws marked ②⑤ (Fig. 7)

## 9. CNシートの外し方

- 9-1. 底板Ass'yを外します。(1項参照)
- 9-2. DM1シートとDM2シートを外します。(2、3項参照)
- 9-3. DM2シートの下側にある、絶縁シートを外します。
- 9-4. DM1シールドシートとDM2シールドシートを手前に起こします。(図 4)
- 9-5. ②⑤ のネジ6本を外しコネクターを抜いて、CNシートを取り外します。(図 5)

## 10. スロットユニットの外し方

- 10-1. 底板Ass'yを外します。(1項参照)
- 10-2. DM1シートとDM2シートを外します。(2、3項参照)
- 10-3. CNシートを外します。(9項参照)
- 10-4. ②⑤ のネジ4本を外して、スロットユニットを取り外します。(図 7)



②⑤ : 4.0×10 Bind Head Tapping Screw (バインドタッピングネジ)

(Fig. 7)

## 11. PNAB and PNC Circuit Boards Removal

- 11-1. Pull out the knobs on the control panel.
- 11-2. Remove the bottom cover assembly. (see procedure 1)
- 11-3. Remove the DM1 and DM2 circuit boards. (see procedures 2 and 3)
- 11-4. Remove the power supply assembly. (see procedure 4)
- 11-5. Remove the keyboard assembly. (see procedure 7)
- 11-6. Remove the sixteen (16) screws marked ②④ to remove the center angle bracket with the DM1, DM2 and MK shield sheets. (Fig. 8)
- 11-7. Remove the CN circuit board. (see procedure 9)
- 11-8. Remove the slot unit. (see procedure 10)

## 11. PNABシートとPNCシートの外し方

- 11-1. パネル表側より、スライドボリューム類のつまみを抜き取っておきます。
- 11-2. 底板Ass'yを外します。(1項参照)
- 11-3. DM1シートとDM2シートを外します。(2、3項参照)
- 11-4. 電源Ass'yを外します。(4項参照)
- 11-5. 鍵盤Ass'yを外します。(7項参照)
- 11-6. ②④ のネジ16本を外して、DM1シールドシート、DM2シールドシート、MKシールドシートと一緒にセンターアングルを外します。(図 8)
- 11-7. CNシートを外します。(9項参照)
- 11-8. スロットユニットを外します。(10項参照)

### 11-9. PNAB circuit board removal

11-9-1. Remove the three (3) screws marked ②⑥① to remove the card guide with the JK (CARD) circuit board. (Fig. 5)

11-9-2. After the six (6) screws marked ①⑨① have been removed, the PNAB circuit board can be removed. (Fig. 9)

\* The PNAB circuit board is connected to the PNC circuit board with connector assembly.

### 11-10. PNC circuit board removal

11-10-1. Remove the two (2) screws marked ②③① to remove the PNC shield sheet. (Fig. 9)

11-10-2. After the six (6) screws marked ②⑦① have been removed, the PNC circuit board can be removed. (Fig. 10)

### 11-9. PNABシートの外し方

11-9-1. ②⑥① のネジ3本を外して、JK(CARD)シートと一緒にカードガイドを取り外します。(図 5)

11-9-2. ①⑨① のネジ6本を外して、PNABシートを取り外します。(図 9)

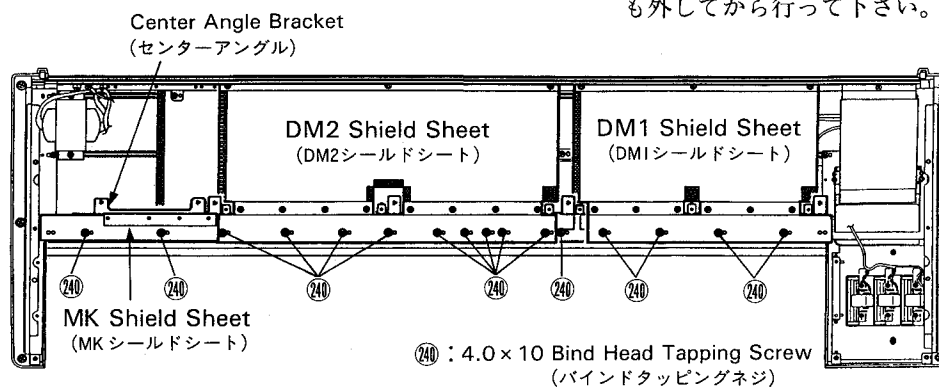
※コネクターも一緒に外す場合は、PNCシートも外してから行って下さい。

### 11-10. PNCシートの外し方

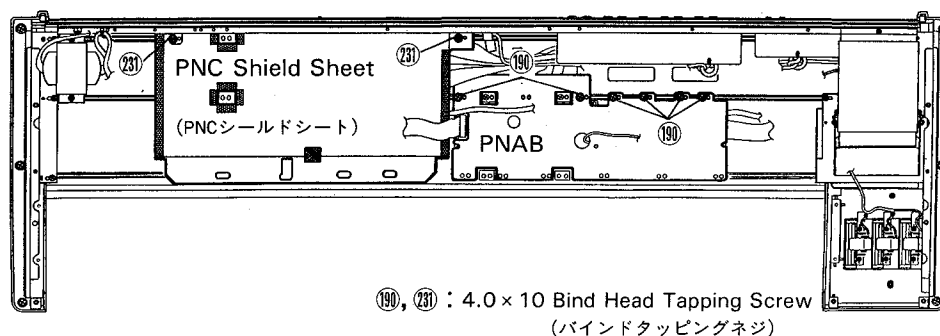
11-10-1. ②③① のネジ2本を外して、PNCシールドシートを外します。(図 9)

11-10-2. ②⑦① のネジ6本を外して、PNCシートを取り外します。(図10)

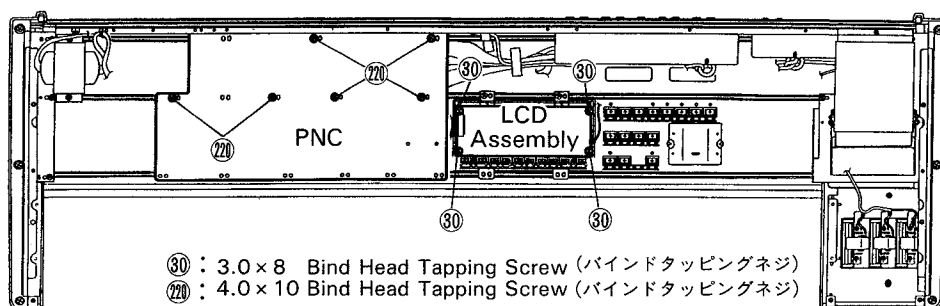
※コネクターも一緒に外す場合は、PNABシートも外してから行って下さい。



(Fig. 8)



(Fig. 9)



(Fig. 10)

## 12. LCD Assembly Removal

- 12-1. Remove the bottom cover assembly. (see procedure 1)
- 12-2. Remove the DM1 and DM2 circuit boards. (see procedures 2 and 3)
- 12-3. Remove the power supply assembly. (see procedure 4)
- 12-4. Remove the keyboard assembly. (see procedure 7)
- 12-5. Remove the CN circuit board. (see procedure 9)
- 12-6. Remove the slot unit. (see procedure 10)
- 12-7. Remove the PNAB circuit board. (see procedure 11-9)
- 12-8. The LCD assembly can be removed by removing the four (4) screws marked ③⑩. (Fig. 10)

## 13. Wheel Assembly Removal

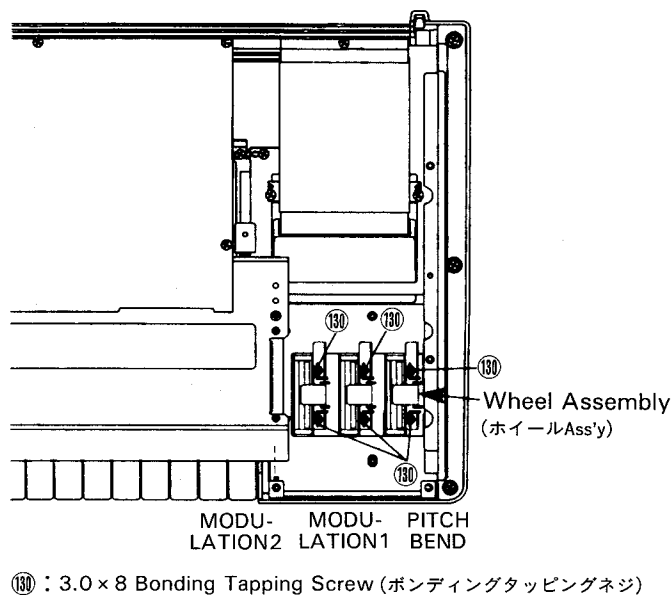
- 13-1. Remove the bottom cover assembly. (see procedure 1)
- 13-2. After the six (6) screws marked ③⑩ have been removed, the wheel assembly can be removed. (Fig. 11)

## 12. LCD Ass'yの外し方

- 12-1. 底板Ass'yを外します。(1項参照)
- 12-2. DM1シートとDM2シートを外します。(2、3項参照)
- 12-3. 電源Ass'yを外します。(4項参照)
- 12-4. 鍵盤Ass'yを外します。(7項参照)
- 12-5. CNシートを外します。(9項参照)
- 12-6. スロットユニットを外します。(10項参照)
- 12-7. PNABシートを外します。(11-9項参照)
- 12-8. ③⑩のネジ4本を外して、LCD Ass'yを取り外します。  
(図10)

## 13. ホイールAss'yの外し方

- 13-1. 底板Ass'yを外します。(1項参照)
- 13-2. ③⑩のネジ6本を外して、ホイールAss'yを取り外します。(図11)



(Fig. 11)



**14. Rotary Encoder Knob Removal**

- 14-1. Remove the bottom cover assembly. (see procedure 1)
- 14-2. Remove the DM1 and DM2 circuit boards. (see procedures 2 and 3)
- 14-3. Remove the power supply assembly. (see procedure 4)
- 14-4. Remove the keyboard assembly. (see procedure 7)
- 14-5. Remove the CN circuit board. (see procedure 9)
- 14-6. Remove the slot unit. (see procedure 10)
- 14-7. Remove the PNC circuit board. (see procedure 11-10)
- 14-8. Pull out the rotary encoder knob on the PNC circuit board.

**14. ロータリーエンコーダツマミ(データエントリーツマミ)の外し方**

- 14-1. 底板Ass'yを外します。(1項参照)
- 14-2. DM1シートとDM2シートを外します。(2、3項参照)
- 14-3. 電源Ass'yを外します。(4項参照)
- 14-4. 鍵盤Ass'yを外します。(7項参照)
- 14-5. CNシートを外します。(9項参照)
- 14-6. スロットユニットを外します。(10項参照)
- 14-7. PNCシートを外します。(11-10項参照)
- 14-8. PNCシートからロータリーエンコーダツマミを取り外します。

# **LSI PIN DESCRIPTION (LSI端子機能表)**

## **• H8/532 (X1722D00) CPU**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	XTAL	I	Clock	43	A8	O	Address bus
2	Vss	I	Ground	44	A9	O	
3	P10/ $\phi$	O	System clock	45	A10	O	
4	P11/E	O	Enable	46	A11	O	
5	P12	O	(Bus acknowledge)	47	A12	O	
6	P13	I	(Bus request)	48	A13	O	
7	P14/WAIT	I	Wait	49	A14	O	
8	P15/IROO	I	Interrupt request 0	50	A15	O	
9	P16/IROI	I	Interrupt request 1	51	A16	O	
10	P17	O	8-bit timer output	52	A17	O	
11	AS	O	Address strobe	53	A18	O	Power supply
12	R/W	O	Read/Write	54	A19	O	
13	DS	O	Data strobe	55	Vcc		
14	RD	O	Read control	56	P70	I/O	
15	WR	O	Write control	57	P71	I/O	
16	Vcc		Power supply	58	P72	I/O	Port 7
17	MD0	I	Mode control	59	P73	I/O	
18	MD1	I		60	P74	I/O	
19	MD2	I		61	P75	I/O	
20	STBY	I	Standby	62	P76	I/O	
21	RES	I	Reset	63	P77	I/O	Ground
22	NMI	I	Non-maskable interrupt	64	Vss		
23	NC			65	AVss		Analog ground
24	Vss		Ground	66	AN0	I	
25	D0	I/O	Data bus	67	AN1	I	Port 8
26	D1	I/O		68	AN2	I	
27	D2	I/O		69	AN3	I	
28	D3	I/O		70	AN4	I	
29	D4	I/O		71	AN5	I	
30	D5	I/O		72	AN6	I	
31	D6	I/O		73	AN7	I	Analog power supply
32	D7	I/O		74	AVcc		
33	A0	O	Address bus	75	P90	I/O	Port 9
34	A1	O		76	P91	I/O	
35	A2	O		77	P92	I/O	
36	A3	O		78	P93	I/O	
37	A4	O		79	P94	I/O	
38	A5	O		80	TXD	I/O	(Transmit data)
39	A6	O		81	RXD	I	(Receive data)
40	A7	O		82	P97	I/O	Ground
41	Vss		Ground	83	Vss		
42	Vss			84	EXTAL	I	Clock

## **• HD63C01Y0F64P (XF148A00) CPU**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	Vss	I	Ground	33	Vcc		DC Supply (+5V)
2	XTAL	I	Clock (8MHz)	34	A15	O	Address bus
3	EXTAL	I		35	A14	O	
4	MP0	I	Mode program	36	A13	O	
5	MP1	I		37	A12	O	
6	RES	I	Reset	38	P11	O	
7	STBY	I	Stand-by mode signal	39	P10	O	Ground
8	NMI	I	Non-maskable interrupt	40	A9	O	
9	P20	I/O	Port 2	41	A8	O	
10	P21	I/O		42	Vss		
11	P22	I/O		43	A7	O	
12	P23	I/O		44	A6	O	
13	P24	I/O		45	A5	O	Address bus
14	P25	I/O		46	A4	O	
15	P26	I/O		47	A3	O	
16	P27	I/O		48	A2	O	
17	P50	I/O	Port 5	49	A1	O	
18	P51	I/O		50	A0	O	Data bus
19	P52	I/O		51	D7	I/O	
20	P53	I/O		52	D6	I/O	
21	P54/IS	I/O		53	D5	I/O	
22	P55/OS	I/O		54	D4	I/O	
23	P56	I/O		55	D3	I/O	
24	P57	I/O	Port 6	56	D2	I/O	
25	P60	I/O		57	D1	I/O	
26	P61	I/O		58	D0	I/O	
27	P62	I/O		59	BA	O	Bus available
28	P63	I/O		60	LIR	O	Load instruction resistor
29	P64	I/O		61	R/W	O	Read/Write control
30	P65	I/O		62	WR	O	Write
31	P66	I/O		63	RD	O	Read
32	P67	I/O		64	E	O	Enable

• **YM3029 (XF237A00) AFDO (Floating Point Converter)**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	DVDD		Digital power supply (+5V)	15	SHA	I	Sample and hold input (Channel A)
2	LE	O	Latch enable	16	EXG		Exponent ground
3	DAB	O	Channel A/B data output	17	EXG		
4	SYW	I	Sync pulse	18	EXI	I	Exponent input
5	CLK	I	Clock	19	EXO	O	Exponent output
6	$\phi 1$	O	Clock for DAC	20	AVSS		Analog power supply (-5V)
7	DGND		Digital ground	21	AVDD		Analog power supply (+5V)
8	AVDD		Analog power supply (+5V)	22	SI1	I	Serial data input 1 (Channel A)
9	AVSS		Analog power supply (-5V)	23	VLA0	I	Volume level select (Channel A)
10	SHB	I	Sample and hold input (Channel B)	24	VLA1	I	
11	CH4	O	Output (Channel 4)	25	SI2	I	Serial data input 2 (Channel B)
12	CH3	O	Output (Channel 3)	26	VLB0	I	Volume level select (Channel B)
13	CH2	O	Output (Channel 2)	27	VLB1	I	
14	CH1	O	Output (Channel 1)	28	4/2	I	Channel number select (4 or 2-channel)

• **YM3422B (XE862B00) ESI**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	Vss		Ground	9	M0	I	Mode select
2	SI0	I	Serial data input 0	10	M1	I	
3	SO0	O	Serial data output 0	11	M2	I	
4	BC0	I	Clock CH0	12	M3	I	
5	WC0	I	W-clock CH1	13	WC1	I	W-clock CH1
6	SI2	I	Serial data input 2	14	BC1	I	Clock CH1
7	SO2	O	Serial data output 2	15	SO1	O	Serial data output 1
8	VDD		Power supply	16	SI1	I	Serial data input 1

• **YM3807 (XA902001) MOD (Modulation Signal Generator)**

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	NC		Inputs data to add to the waveform data inside MOD	24	Vss		Power supply ground
2	MDSI0	I		23	CDO	O	CD interface serial data output
3	MDSI1	I		22	CDI	I	CD interface serial data input
4	MDSO0	O		21	NC		CD interface transmission clock input
5	MDSO1	O		20	XCLK	I	
6	MOD0	O	Outputs MOD internal waveform data with the same data format as MDSIO.	19	XMD	I	Selects 1/16 mode (asynchronous) or 1/1 mode (synchronous) for the CD interface
7	MOD1	O		18	$\overline{\text{CRS}}$	I	CD counter reset
8	MOD2	O		17	CLK	I	Clock
9	MOD3	O		16	$\overline{\text{IC}}$	I	Initial clear
10	MOD4	O		15	SYW	I	Sync signal input. One 64th of the master clock.
11	MOD5	O	Outputs waveform data for all channels inside MOD.	14	MOD7	O	Outputs waveform data for all channels inside MOD.
12	VDD		Power supply (+5V)	13	MOD6	O	

## • YM6007 (XF164A00) DSP 2 (Digital Signal Processor)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	D18	I/O	Data bus	65	NC		
2	D17	I/O		66	CDO	O	Serial control data output
3	D16	I/O		67	CDI	I	Serial control data input
4	NC		Power supply	68	VDD		Power supply
5	VDD			69	SIO	I	Serial data input (28bit × 4ch)
6	D15	I/O		70	NC		
7	NC		Data bus	71	NC		
8	NC			72	SI1	I	Serial data input (28bit × 4ch)
9	D14	I/O		73	SI2	I	Serial data input (28bit × 2ch)
10	NC			74	SO0	O	Serial data output (28bit × 4ch)
11	D13	I/O		75	NC		
12	D12	I/O		76	SO1	O	Serial data output (28bit × 4ch)
13	D11	I/O		77	SO2	O	Serial data output (28bit × 2ch)
14	NC			78	SCLK	O	Clock (64bit/sample)
15	D10	I/O		79	NC		
16	NC			80	NC		
17	NC			81	NC		
18	D9	I/O		82	NC		
19	D8	I/O		83	TRGO	O	Trigger output
20	D7	I/O		84	TRGI	I	Trigger input
21	NC			85	DCLK	I	Clock (Master clock × 2)
22	D6	I/O	Address bus	86	SYW	I	Synch. pulse
23	D5	I/O		87	IC	I	Initial clear
24	NC			88	NC		
25	D4	I/O		89	MRQ	O	Control data receive
26	NC			90	MDA0	I	
27	D3/A15	I/O		91	NC		
28	NC			92	NC		Serial mode: Internal register select
29	D2/A14	I/O		93	MDA1	I	Parallel mode: CDI, CDO data format select
30	D1/A13	I/O		94	MDA2	I	
31	D0/A12	I/O		95	NC		
32	NC			96	MWE	I	MD pin input strobe
33	CAS/A11	O		97	MOE	I	MD pin output strobe
34	RAS/A10	O		98	MOS	I	Communication mode select (0: serial 1: parallel)
35	A9	O	Address bus	99	DM7	I/O	Parallel data
36	A8	O		100	DM6	I/O	
37	VSS			101	NC		
38	A7	O		102	NC		
39	NC			103	DM5	I/O	
40	A6	O		104	NC		
41	NC			105	DM4	I/O	
42	A5	O		106	NC		
43	NC			107	DM3	I/O	
44	A4	O		108	DM2	I/O	
45	A3	O		109	DM1	I/O	
46	NC			110	DM0	I/O	
47	NC			111	NC		
48	NC			112	NC		
49	NC			113	D27	I/O	
50	NC			114	NC		
51	NC			115	D26	I/O	
52	A2	O	Memory data bus	116	NC		
53	A1	O		117	D25	I/O	
54	A0	O		118	D24	I/O	
55	WE	O		119	NC		
56	OE	O		120	D23	I/O	
57	NC			121	NC		
58	DBOE	I		122	NC		
59	NC			123	D22	I/O	
60	TIM1	O		124	VSS		
61	TST			125	NC		
62	CRS	I/O		126	D21	I/O	
63	NC			127	D20	I/O	
64	XCLK	I		128	D19	I/O	

• **YM7102 (XG996A00) PAN (Panning Processor)**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	A0	I	Address bus	41	L8/ACC8	O	L channel data
2	D7	I/O		42	L9/ACC9	O	
3	D6	I/O		43	L10/ACC10	O	
4	D5	I/O	Data bus	44	L11/ACC11	O	
5	D4	I/O		45	L12/ACC12	O	
6	D3	I/O		46	L13/ACC13	O	
7	D2	I/O		47	L14/ACC14	O	
8	D1	I/O		48	L15/ACC15	O	
9	D0	I/O		49	R0/ACC16	O	R channel data
10	IN1	I	Data from OPS	50	R1/ACC17	O	
11	IN0	I	Data from PAN (cathcade input)	51	R2/ACC18	O	
12	SI2	I		52	R3/ACC19	O	
13	SI1	I		53	R4	O	
14	TEGSS	I	Test pin	54	R5	O	
15	TEGS2	I		55	R6	O	
16	TEGS1	I		56	R7	O	
17	TEGSO	I		57	R8	O	
18	NC		Control data for DSP	58	R9	O	
19	CDO	O		59	R10	O	
20	CRS	O		60	R11	O	Address bus
21	S1	O	Signal to DSP	61	R12	O	
22	S2	O		62	R13	O	
23	SYW	O	Sync pulse for DSP	63	R14	O	
24	DSPCLK	O	Clock for DSP	64	R15	O	
25	MODE	I	Output mode (L:16bits DAC H:20bits DAC)	65	NC		
26	IC	I	Initial clear	66	TTIM	I	
27	SYNC	I	Sync pulse	67	TEG1	I	
28	$\phi M$	I	Clock	68	TEGO	I	
29	V <sub>SE</sub>		Ground	69	TRD	I	
30	V <sub>SS</sub>			70	CS2	I	Chip select
31	V <sub>DD</sub>		Power supply	71	CS1	I	
32	V <sub>DD</sub>			72	V <sub>DD</sub>		Power supply
33	L0/ACC0	O		73	CS0	I	
34	L1/ACC1	O		74	A7	I	Address bus
35	L2/ACC2	O	L channel data	75	A6	I	
36	L3/ACC3	O		76	A5	I	
37	L4/ACC4	O		77	A4	I	
38	L5/ACC5	O		78	A3	I	
39	L6/ACC6	O		79	A2	I	
40	L7/ACC7	O		80	A1	I	

• **μPD71055C (XB361001) PPI (Programmable Peripheral Interface)**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	PO3	I/O	Port 0	21	P13	I/O	Port 2
2	PO2	I/O		22	P14	I/O	
3	PO1	I/O		23	P15	I/O	
4	PO0	I/O		24	P16	I/O	
5	RD	I	Read control	25	P17	I/O	DC Supply
6	CS	I	Chip Select	26	V <sub>DD</sub>		
7	GND		DC Supply (0V)	27	D7	I/O	Data bus
8	A1	I	Port address	28	D6	I/O	
9	A0	I		29	D5	I/O	
10	P27	I/O		30	D4	I/O	
11	P26	I/O	Port 2	31	D3	I/O	
12	P25	I/O		32	D2	I/O	
13	P24	I/O		33	D1	I/O	
14	P20	I/O		34	D0	I/O	
15	P21	I/O		35	RESET	I	Reset
16	P22	I/O	Port B	36	WR	I	Write control
17	P23	I/O		37	PO7	I/O	Port 0
18	P10	I/O		38	PO6	I/O	
19	P11	I/O		39	PO5	I/O	
20	P12	I/O		40	PO4	I/O	

• **YM7103 (XG993A00) EGM2 (Envelope Generator)**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	A0	I	Address bus	41	NC		
2	D7	I/O		42	KON	O	Key on data
3	D6	I/O		43	E0	O	
4	D5	I/O		44	E1	O	
5	D4	I/O		45	E2	O	
6	D3	I/O	Data bus	46	E3	O	
7	D2	I/O		47	E4	O	
8	D1	I/O		48	E5	O	
9	D0	I/O		49	E6	O	Envelope data, Pitch data (porta- ment), Pitch envelope data
10	NC			50	E7	O	
11	TST10	O		51	E8	O	
12	TST9	O		52	E9	O	
13	TST8	O		53	E10	O	
14	TST7	O		54	E11	O	
15	TST6	O		55	E12	O	
16	TST5	O	Test pin	56	E13	O	
17	TST4	O		57	NC		
18	TST3	O		58	NC		
19	TST2	O		59	NC		
20	TST1	O		60	NC		
21	TST0	O		61	NC		
22	$\phi$ M0	O	Clock	62	NC		
23	XTAL	O	Quartz crystal	63	NC		
24	EXTAL	I		64	NC		
25	IC	I	Initial clear	65	NC		
26	SYO	O	Sync pulse	66	NC		
27	SYI	I	Sync pulse	67	NC		
28	$\phi$ M1	I	Clock	68	NC		
29	Vss		Ground	69	NC		
30	Vss			70	NC		
31	NC			71	TRD	I	Test pin
32	VDD		Power supply	72	VDD		Power supply
33	NC			73	CS0	I	
34	NC			74	CS1	I	Chip select
35	NC			75	CS2	I	
36	TEGS2	I		76	A5	I	
37	TEGS1	I	Test pin	77	A4	I	
38	TEGS0	I		78	A3	I	Address bus
39	TS01	O	Test pin	79	A2	I	
40	TS00	O		80	A1	I	

• **WD37C65C-JM00 (XH129B00) FDC (Floppy Disk Controller)**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	RD	I	Read control	23	XT2	I	XTAL osc. in
2	WR	I	Write control	24	DRV	I	Drive type
3	CS	I	Chip select	25	XT1	O	XTAL osc. drive
4	A0	I	Register select	26	XT1	I	XTAL osc. in
5	DACK	I	DMA acknowledge	27	PCVAL	I	Precompensation value
6	TC	I	Terminal Count	28	HS	O	Head select (Side select)
7	DB0	I/O		29	WE	O	Write enable
8	DB1	I/O		30	WD	O	Write data
9	DB2	I/O		31	DIRC	O	Direction control
10	DB3	I/O	Data bus	32	STEP	O	Step pulse
11	DB4	I/O		33	DS1	O	Drive select 1
12	DB5	I/O		34	Vss		Ground
13	DB6	I/O		35	DS2	O	Drive select 2
14	DB7	I/O		36	MO1/DS3	O	Motor ON 1/Drive select 3
15	DMA	O	Direct memory access request	37	MO2/DS4	O	Motor ON 2/Drive select 4
16	IRQ	O	Interrupt request	38	HDL	O	Head loaded
17	DCHGEN	I	Disk change enable	39	RPM/RWC	O	Revolutions per minute/Reduced write current
18	LDOR	I	Load operations register	40	DCHG	I	Disk change
19	LDOR	I	Load control register	41	WP	I	Write protected
20	RST	I	Reset	42	TROO	I	Track 00 signal
21	RDD	I	Read disk data	43	IDX	I	Index
22	XT2	O	XTAL osc. drive	44	Vcc		Power supply

• **YM7107 (XG994A00) OPS3 (FM Tone Generator)**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	A0	I	Address bus	41	DA8	O	D/A signal (straight binary)
2	D7	I/O		42	DA9	O	
3	D6	I/O		43	DA10	O	
4	D5	I/O	Data bus	44	DA11	O	
5	D4	I/O		45	DA12	O	
6	D3	I/O		46	DA13	O	(MSB)
7	D2	I/O		47	DA14	O	
8	D1	I/O		48	DA15	O	
9	D0	I/O	Envelope data, Pitch envelope data, Pitch data	49	SH1	O	Sample and hold
10	E13	I		50	SH2	O	
11	E12	I		51	SC0	O	Channel distribution
12	E11	I		52	SC1	O	
13	E10	I		53	SC2	O	Serial data (2 compl. 16bits LSB first)
14	E9	I	Phase reset for phase accumulator Initial clear	54	SO0	O	
15	E8	I		55	SO1	O	
16	E7	I		56	NC		Serial data
17	E6	I		57	NC		
18	E5	I		58	NC		
19	E4	I	Sync pulse (127C127) Clock	59	NC		
20	E3	I		60	NC		Power supply
21	E2	I		61	NC		
22	E1	I		62	NC		Chip select
23	E0	I		63	NC		
24	KON	I	Ground	64	NC		Address bus
25	IC	I		65	NC		
26	NC		Power supply (LSB)	66	NC		Ground
27	SYNC	I		67	NC		
28	$\phi M$	I	D/A signal (straight binary)	68	Vss		Power supply
29	Vss			69	S10	I	
30	Vss		D/A signal (straight binary)	70	S11	I	Power supply
31	VDD			71	NC		
32	VDD		D/A signal (straight binary)	72	VDD		Chip select
33	DA0	O		73	CS0	I	
34	DA1	O	D/A signal (straight binary)	74	CS1	I	Address bus
35	DA2	O		75	CS2	I	
36	DA3	O	D/A signal (straight binary)	76	A4	I	Ground
37	DA4	O		77	A3	I	
38	DA5	O	D/A signal (straight binary)	78	A2	I	Ground
39	DA6	O		79	A1	I	
40	DA7	O	D/A signal (straight binary)	80	Vss		

• **HD63B01Y0RM21P (XG950C00) CPU (PKS)**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	Vss		Ground	33	Vcc		DC Supply (+5V)
2	XTAL	I	Clock (8MHz)	34	P47	O	Port 4
3	EXTAL	I		35	P46	O	
4	MP0	I	Mode program	36	P45	O	
5	MP1	I		37	P44	O	
6	RES	I	Reset	38	P43	O	
7	STBY	I	Stand-by mode signal	39	P42	O	Ground
8	NMI	I	Non-maskable interrupt	40	P41	O	
9	P20	I/O	Port 2	41	P40	O	
10	P21	I/O		42	Vss		
11	P22	I/O		43	P17	O	
12	P23	I/O		44	P16	O	Port 1
13	P24	I/O		45	P15	O	
14	P25	I/O	Port 5	46	P14	O	
15	P26	I/O		47	P13	O	
16	P27	I/O		48	P12	O	
17	P50	I/O	Port 6	49	P11	O	Port 3
18	P51	I/O		50	P10	O	
19	P52	I/O		51	P37	I/O	
20	P53	I/O		52	P36	I/O	
21	P54	I/O		53	P35	I/O	Port 7
22	P55	I/O	Port 3	54	P34	I/O	
23	P56	I/O		55	P33	I/O	
24	P57	I/O		56	P32	I/O	
25	P60	I/O		57	P31	I/O	
26	P61	I/O	Port 6	58	P30	I/O	Enable
27	P62	I/O		59	P74	O	
28	P63	I/O		60	P73	O	
29	P64	I/O		61	P72	O	
30	P65	I/O		62	P71	O	
31	P66	I/O	Port 6	63	P70	O	
32	P67	I/O		64	E	O	

• YM7119 (XG995A00) M3 (AWM Tone generator & Digital Filter)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	INDV0	O	Individual output 0 (8 channels)	65	WA8	O	Wave memory address bus
2	INDV1	O	Individual output 1 (8 channels)	66	WA9	O	
3	OPZ	I	MELIN input select (⊕ OPZ, ⊙ PAN)	67	WA10	O	
4	DIOUT0	O	Stereo output (L & R)	68	WA11	O	
5	DIOUT1	O	Assignable output (ch.0 & ch.4)	69	WA12	O	
6	DIOUT2	O	Assignable output (ch.1 & ch.5)	70	WA13	O	
7	DIOUT3	O	Assignable output (ch.2 & ch.6)	71	WA14	O	
8	DIOUT4	O	Assignable output (ch.3 & ch.7)	72	NC		
9	MELIN	I	MEL formatted signal input	73	WA15	O	
10	LSB/MSB	I	Individual output mode select	74	WA16	O	
11	TTPAD0	I/O	(⊕ MSB first, ⊙ LSB first)	75	WA17	O	CPU address bus
12	TTPAD1	I/O		76	WA18	O	
13	NC		Test pin	77	WA19	O	
14	TTPAD2	I/O		78	WA20	O	
15	TTPAD3	I/O		79	WA21	O	
16	TTPAD4	I/O		80	WA22	O	
17	TTPAD5	I/O		81	WA23	O	
18	NC			82	A0	I	
19	TTPAD6	I/O		83	A1	I	
20	TTPAD7	I/O		84	A2	I	
21	NC			85	A3	I	
22	TTPAD8	I/O	Individual input 0 (8 channels) Individual input 1 (8 channels)	86	A4	I	CPU data bus
23	TTPAD9	I/O		87	A5	I	
24	NC			88	D0	I/O	
25	TTPAD10	I/O		89	NC		
26	TTPAD11	I/O		90	D1	I/O	
27	DIIN0	I		91	D2	I/O	
28	DIIN1	I		92	D3	I/O	
29	WD0	I/O		93	D4	I/O	
30	WD1	I/O		94	D5	I/O	
31	WD2	I/O		95	D6	I/O	
32	WD3	I/O	Wave memory data	96	D7	I/O	
33	NC			97	S/HSC0	I	Sample and hold set timing 0~3
34	WD4	I/O		98	S/HSC1	I	
35	WD5	I/O		99	S/HSC2	I	
36	WD6	I/O		100	S/HSC3	I	
37	WD7	I/O		101	S/HEN	O	Sample and hold enable
38	WD8	I/O		102	S/H0	O	Sample and hold 0~3
39	WD9	I/O		103	S/H1	O	
40	NC			104	S/H2	O	
41	NC		Ground Power supply	105	S/HRCA	I	Sample and hold reset A and B
42	WD10	I/O		106	S/HRCB	I	
43	WD11	I/O		107	IC	I	Initial clear
44	NC			108	Vss		Ground
45	WD12	I/O		109	XTAL	O	Clock
46	WD13	I/O		110	EXTAL	I	
47	WD14	I/O		111	NC		Sync. signal on 2 chips mode
48	Vss			112	FCLKOUT	O	
49	VDD			113	FCLKIN	I	6.144MHz clock
50	WD15	I/O	Wave data MSB write signal Wave data LSB write signal Output enable for wave data Odd/Even select on 2 chips mode Wave memory single/dual mode select (⊕ : dual-2 chips mode, ⊙ : single-1 chip mode)	114	NC		
51	MSBW	O		115	CLK3	O	Power supply
52	LSBW	O		116	VDD		
53	OE	O		117	SYWIN	I	Sync. signal for MEL format
54	ODD/EVEN	I		118	CLKMEL	O	3.072MHz clock for MEL format
55	SINGLE/DUAL	I		119	NC		Latch enable for PCM56 (DAC)
56	WA0	O		120	DACLE	O	
57	WA1	O		121	SYWOUT	O	Sync pulse for MEL format
58	WA2	O		122	SYW64	O	6.144MHz sync. signal
59	WA3	O		123	IRO	O	Interrupt request (open drain)
60	WA4	O	Wave memory address bus	124	CS	I	Chip select
61	WA5	O		125	R/W	I	Read/Write control
62	WA6	O		126	CHPIN	I	EG lowest ch. detect
63	WA7	O		127	CHPOUT	O	EG lowest ch. detect
64	NC			128	KSYNC	I	Key on sync. signal from AFM



• TMC57800N (XG662A00) MIX5 (Mixer)

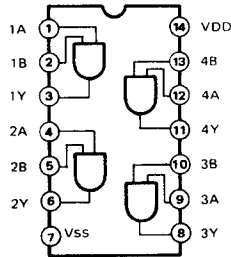
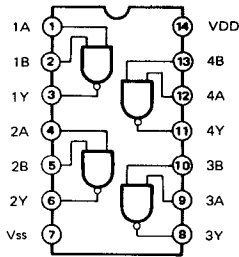
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	MX17	I	Voice data input	11	SYM	I	Synch pulse
2	MX16	I		12	CDO	O	Control data output
3	MX15	I		13	XCLK	I	CDI and CDO in/out clock
4	MX14	I		14	CDI	I	Control data input
5	MX13	I		15	CRS	I	Counter reset for CDI and CDO
6	MX12	I		16	MX00	O	Voice data output
7	MX11	I		17	MX01	O	
8	MX10	I	Master clock	18	MX02	O	
9	CLK	I		19	MX03	O	
10	Vss		Ground	20	VDD		Power supply

• LC9116A-483 (XI364A00) <TW80> Decoder

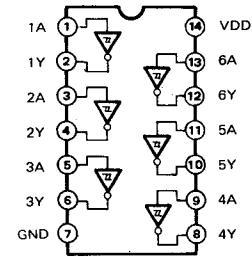
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	MX00	O	Mix output (24-bit limit) MEL (A) (B)	33	Vss		Ground
2	MX01	O		34	RSTB	O	Reset output
3	LIM00	O	Limiter output (22-bit limit) MEL	35	WA17	I	Wave address bus
4	LIM01	O		36	WA18	I	
5	LIM02	O		37	WA19	I	
6	LIM03	O		38	WA20	I	
7	Vss		Ground	39	WA21	I	
8	CO1	O	OR-output (A) (B) (C)	40	WA22	I	Decoder output to WAVE CARD
9	CO2	O		41	WA23	I	
10	CO3	O		42	CARDB	O	
11	AI4	I	Buffer input	43	RAM2B	O	
12	AI3	I		44	RAM1B	O	Decoder output to WAVE RAM
13	AI2	I		45	ROM4B	O	
14	AI1	I		46	ROM3B	O	
15	BI1	I	Inverting input	47	ROM2B	O	Decoder output to WAVE ROM
16	BO1	O	Inverting output	48	ROM1B	O	
17	Vss		Ground	49	Vss		Ground
18	SYW1	I	Synch. signal	50	EXTAL	I	Clock (12.288 MHz)
19	CLK	I	Clock	51	XTAL	I	
20	PST1B	I	Reset input	52	Vss		Ground
21	PST2B	I		53	FCLK	O	Clock (12.288 MHz)
22	AO1	O	Buffer output	54	LCLK2	O	Clock (6.144 MHz)
23	AO2	O		55	LCLK1	O	Clock (6.144 MHz)
24	VDD		Power supply	56	VDD		Power supply
25	AO3	O	Buffer output	57	LIMI3	I	Limiter input (24-bit) MEL
26	AO4	O		58	LIMI2	I	
27	S0	I	OR-input (A)	59	LIMI1	I	
28	S1	I		60	LIMI0	I	Mix input (B)
29	S2	I	OR-input (B)	61	MX13	I	
30	S3	I		62	MX12	I	Mix input (A)
31	S4	I	OR-input (C)	63	MX11	I	
32	S5	I		64	MX10	I	

# ■ IC BLOCK DIAGRAM (ICブロック図)

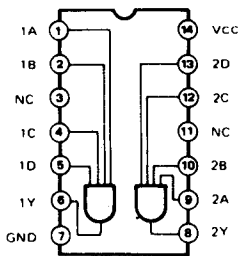
- **TC74HC00AF-TP1** (XD655A00) Quad 2 Input NAND
- **TC74HC08AF-TP1** (XD658A00) Quad 2 Input AND



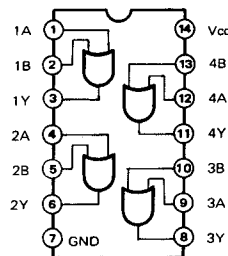
- **SN74HC14N** (IR001450) Hex Inverter
- **SN74LS14N** (IG049650) Hex Inverter



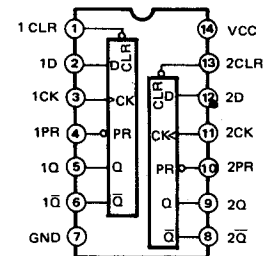
- **TC74HC21AF** (XJ622A00) Dual 4 Input AND



- **SN74ALS32N** (XA055001) Quad 2 Input OR

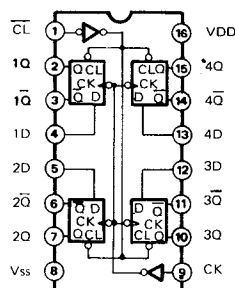
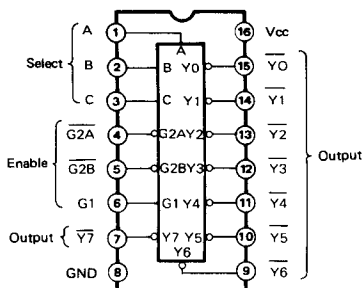


- **SN74HC74NSR** (XC726001) Dual D-Type Flip-Flop

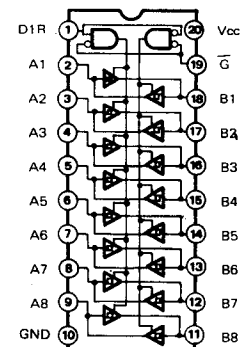


INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	Q̄ <sub>0</sub>

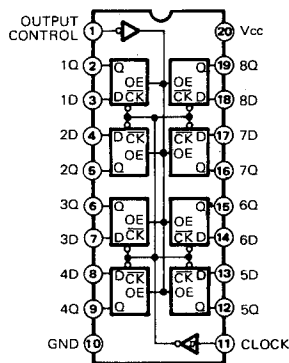
- **SN74ALS138N** (IG149600) 3 to 8 Demultiplexer
- **TC74HC175AF-TP1** (XD658A00) Quad D-Type Flip-Flop



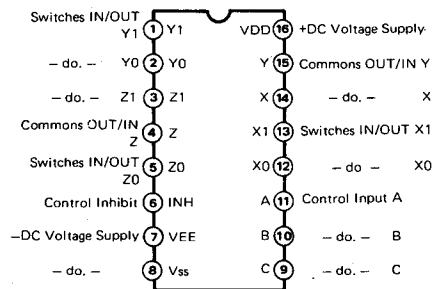
- **SN74ALS245ANSR** (XE057A00) Octal 3-State Bus Transceiver
- **SN74LS245ANSR** (XH779A00) Octal 3-State Bus Transceiver
- **TC74AC245P** (XH608A00) Octal 3-State Bus Transceiver
- **TC74HC245AP** (IR024500) Octal 3-State Bus Transceiver
- **TC74HC245F-T1** (XD603A00) Octal 3-State Bus Transceiver



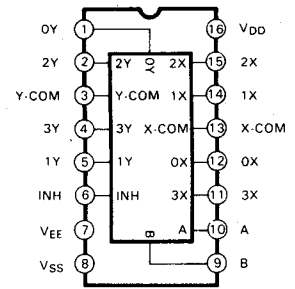
- **SN74HC273N** (IR027350)  
Octal D-Type Flip-Flop



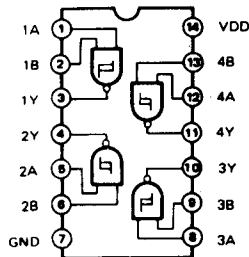
- **TC74HC4051AF** (XJ623A00) • **TC74HC4052AP** (IR405200)  
Single 8-ch.  
Multiplexer/Demultiplexer



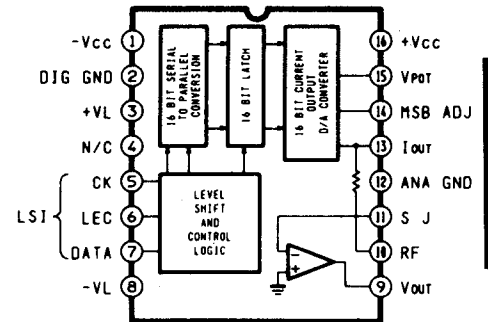
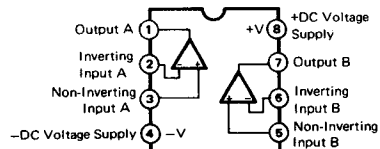
Differential 4-Channel  
Multiplexer/Demultiplexer



- **TC4093BP** (IG043300)  
Quad 2-Input NAND Schmitt Trigger



- **M5238P R610** (XJ748A00) • **PCM56P-Y** (XH690A00)  
Dual Operational Amplifier

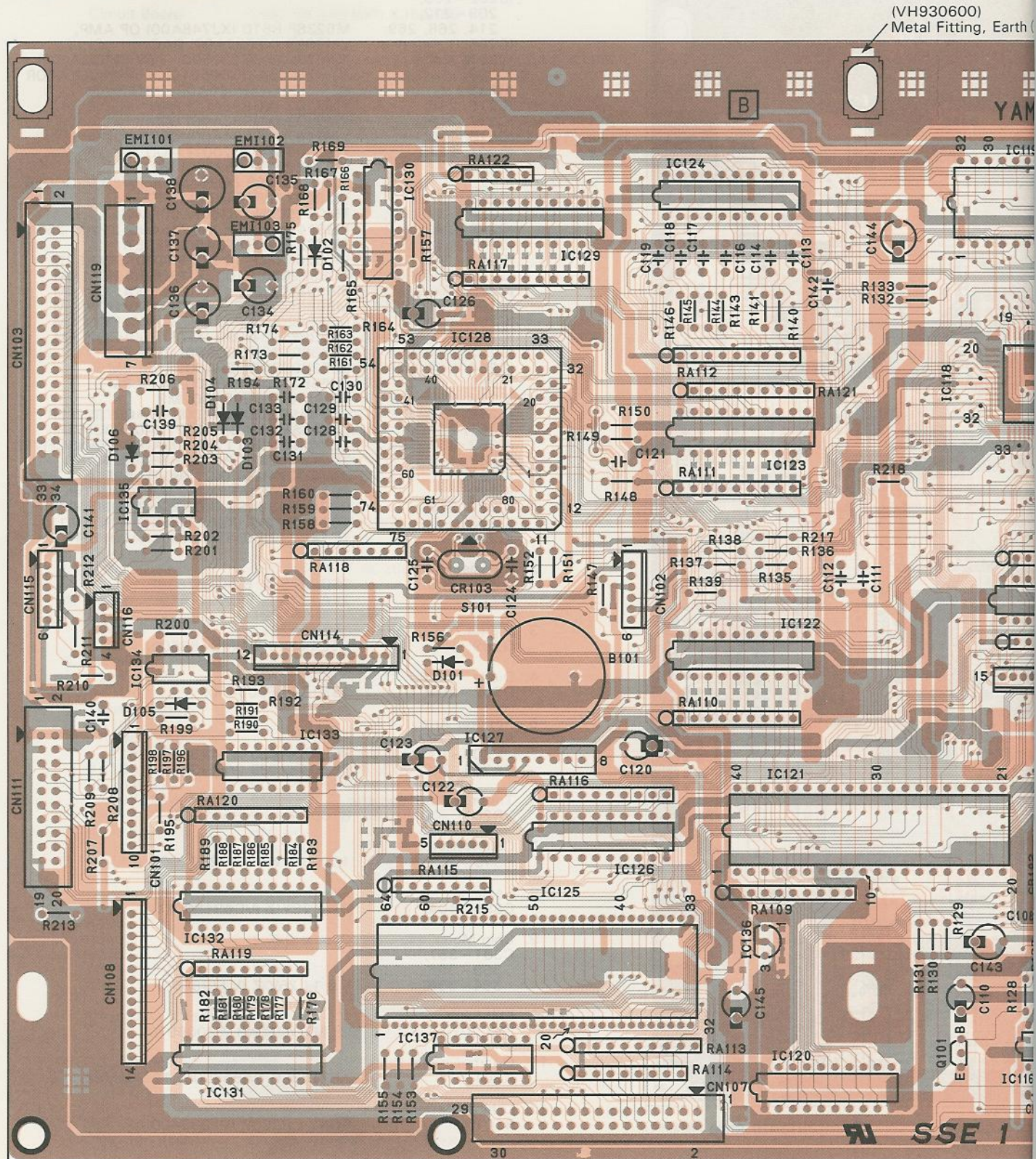


SY99



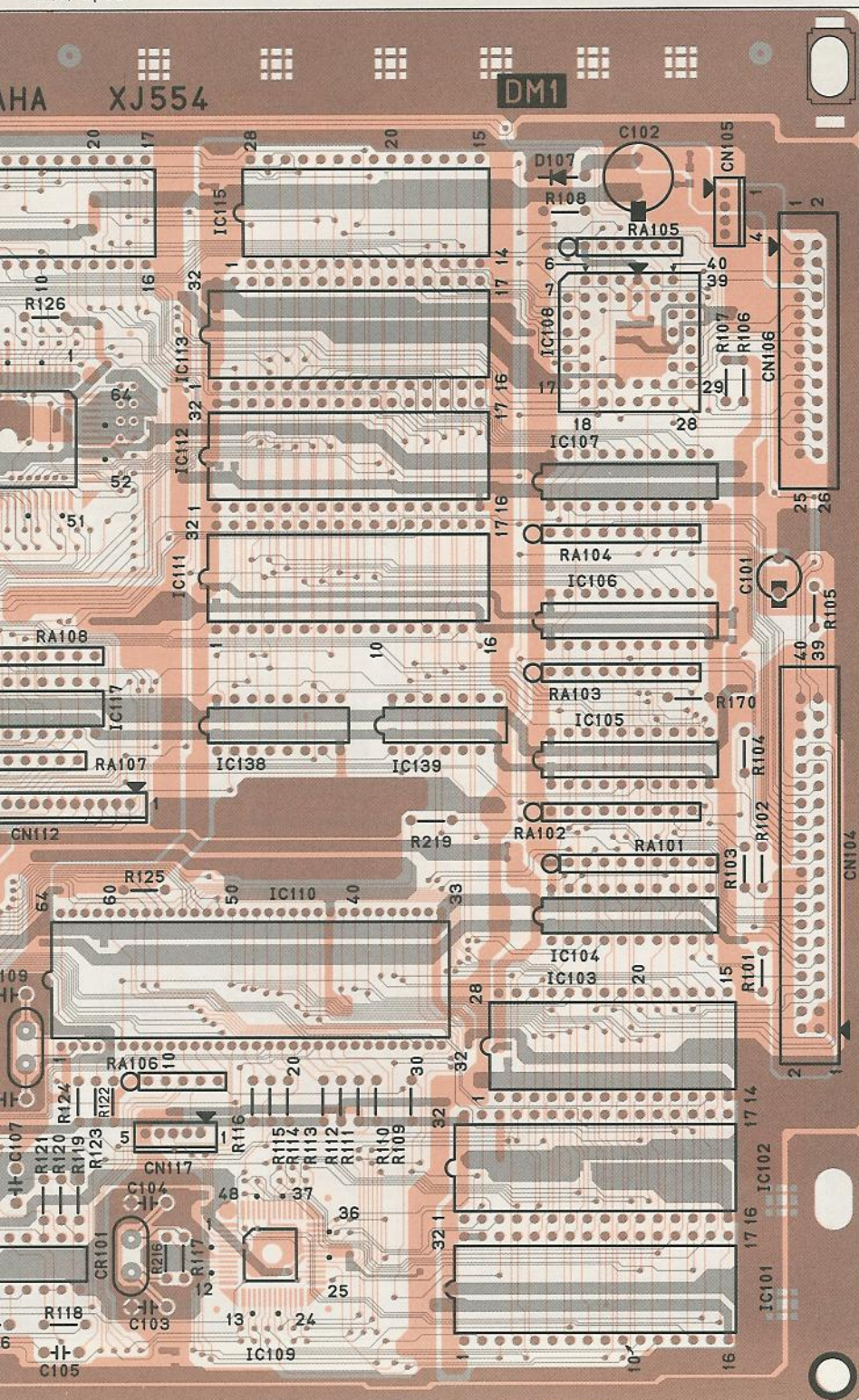
# CIRCUIT BOARDS (シート基板図)

## DM1 Circuit Board





ース金具) 3pcs



Components side (部品側)

Notes)

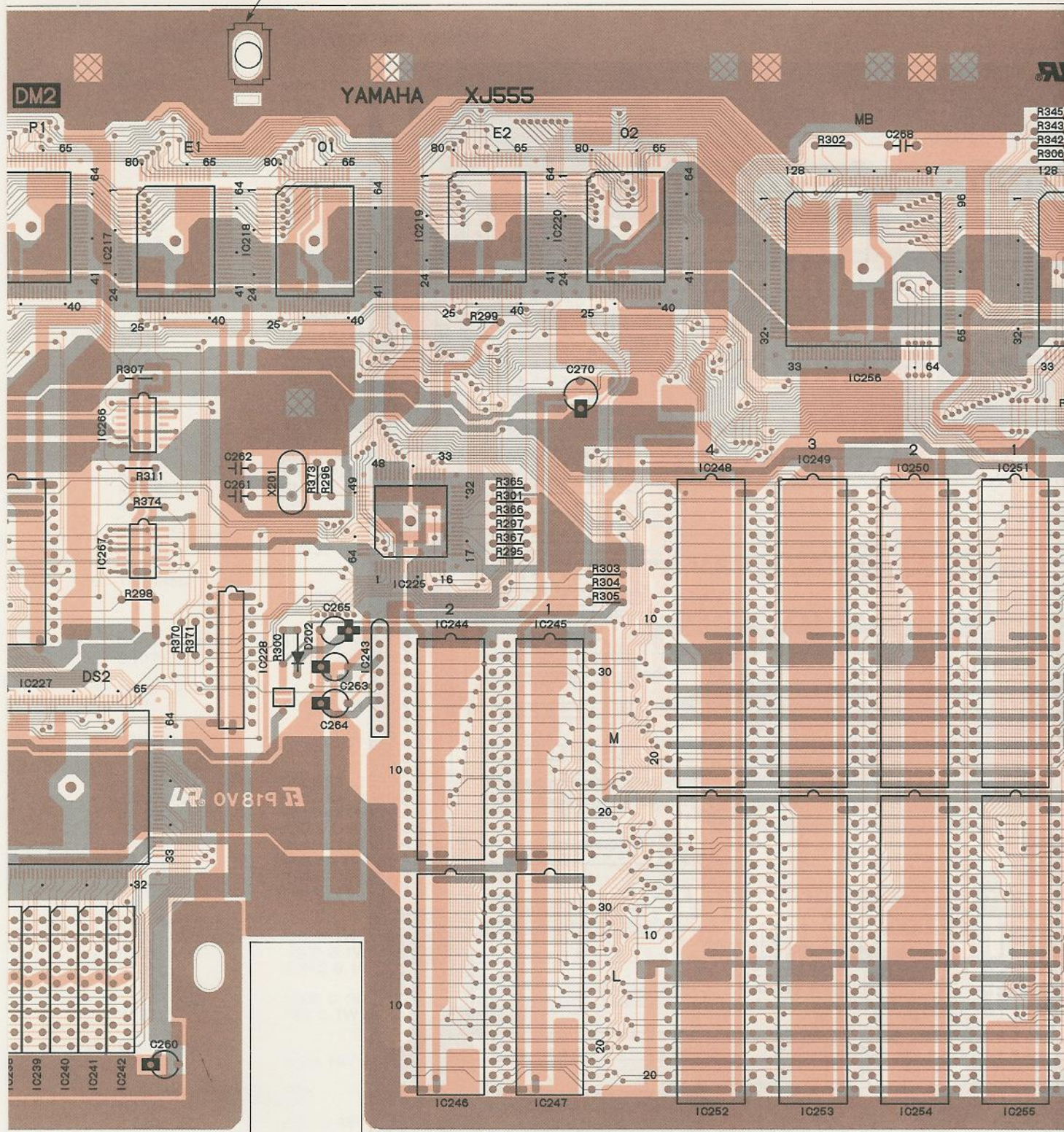
Circuit Board:	DM1 (VK287400) XJ55ABO
1. IC	
IC101:	M5M27C201K (XJ616C00) EPROM (040DV120)
IC102:	HM658128P-12 (XE612A00) PSRAM
IC103:	LH5164D-10L (XF876A00) SRAM
IC104 ~ 107,	
122, 123, 129:	SN74ALS245AN (IG149900) BUS TRANSCEIVER
IC108:	WD37C65C-JM00 (XH129B00) FDD CONTROLLER
IC109:	LZ95A13 (XI501A00) GATE ARRAY
IC110:	HD63C01YOF64P (XF148A00) CPU
IC111:	TC574000D (XJ613D00) EPROM (040AV120)
IC112:	HN27C101AG (XJ614B00) EPROM (040BV110)
IC113:	HN27C101AG (XJ615C00) EPROM (040CV120)
IC115:	HM62256LP-10 (XH266A00) SRAM
IC116:	TC4093BP (IG043300) NAND
IC117, 120, 126,	
131, 132:	TC74HC245AP (IR024500) BUS BUFFER
IC118:	LZ95B12 (XI500A00) GATE ARRAY
IC119:	HM628128LP-10 (XI580A00) SRAM
IC121:	$\mu$ PD71055C (XB361001) PPI
IC124:	TC74AC245P (XH608A00) BUS TRANSCEIVER
IC125:	HD63B01YORM21P (XG950C00) PKS
IC127:	M62021L (XH970A00) RESET
IC128:	H8/532 (XI722D00) CPU
IC130:	TC74HC4052AP (IR405200) MULTIPLEXER
IC133:	SN74LS14N (IG049650) INVERTER
IC135:	RC4558D-V (IG001390) OP AMP.
IC137:	SN74HC14N (IR001450) INVERTER
IC138:	SN74ALS138N (IG149600) DECODER
IC139:	SN74ALS32N (XA055001) OR
2. Photo Coupler	
IC134:	6N137 (VD473200)
3. Transistor	
Q101:	2SC2603 E, F (IC260320)
4. Diode	
D101 ~ 106:	1SS133 (IF003450)
D107:	11ES4 (VB481900)
5. Metal Film Resistor	
R201, 202:	10K $\Omega$ 1/5W F (VA074400)
6. Resistor Array	
RA101 ~ 104,	
108 ~ 112,	
116, 117, 121:	RGLD8X103J (VE445200)
RA105:	RMLS5J102 (VK409500)
RA106, 122:	RGLD4X103J (VE443500)
RA107, 114:	RMLS7J103 (VG284400)
RA113:	RGLD8X223J (VE445400)
RA115:	RMLS6-223J (VA823000)
RA118:	RMLS6J103 (HZ004650)
RA119, 120:	RMLS7153J (VK437400)
7. Chip Resistor	
R301 ~ 303, 324:	47 $\Omega$ 0.1W J (RD254470)
R304, 308:	10K $\Omega$ 0.1W J (RD257100)
R305:	4.7K $\Omega$ 0.1W J (RD256470)
R309 ~ 323,	
325 ~ 332:	100 $\Omega$ 0.1W J (RD255100)
R333:	1K $\Omega$ 0.1W J (RD256100)
8. Electrolytic Cap.	
C102:	470 $\mu$ 16V (UJ838470)
9. Chip Monolithic Cera. Cap.	
C201 ~ 218,	
220 ~ 272:	F 0.1 $\mu$ 25V Z (VJ798800)
10. EMI Filter	
EMI101 ~ 103:	LS MT Y223NB (FZ006970)
11. Quartz Crystal Unit	
CR101:	16MHz AT-49 (VI573400)
CR102:	12MHz AT-49 (VE463500)
CR103:	24MHz AT-49 (VK409400)
12. Lithium Battery	
B101:	SONY/CR2032 (VE338400)



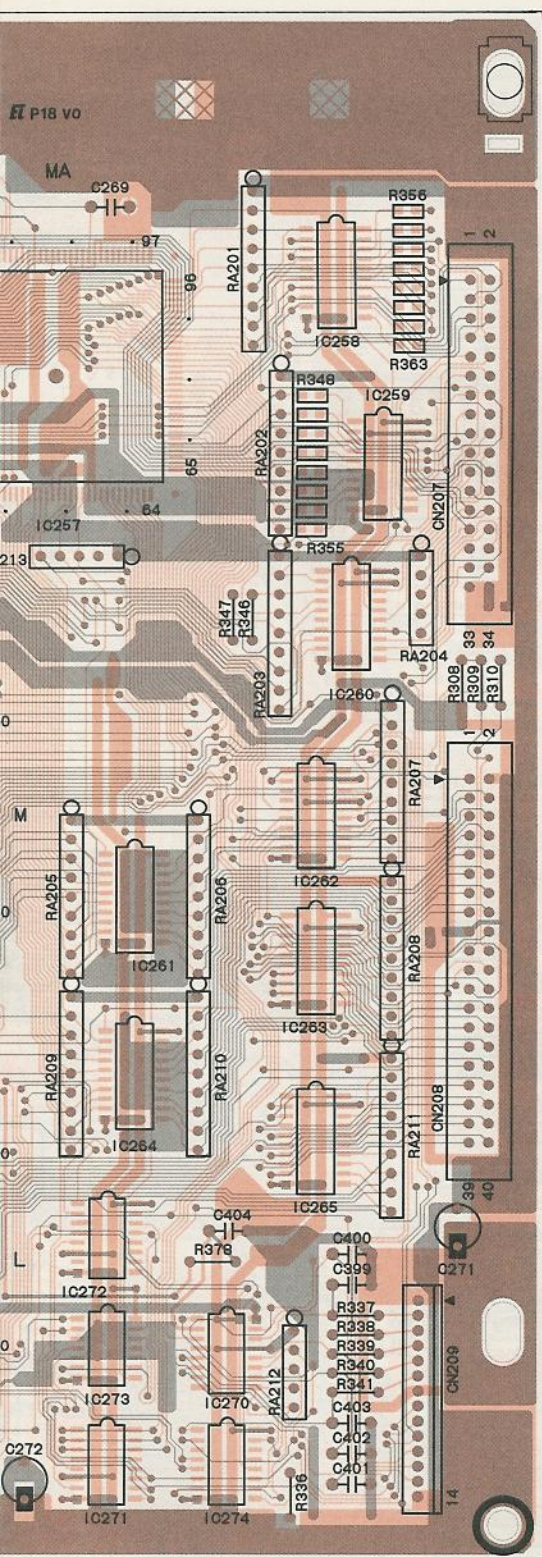




(VH930600)  
Metal Fitting, Earth (アース金具)







Components side (部品側)

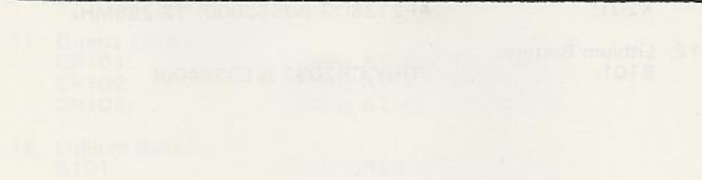
## Notes)

Circuit Board:

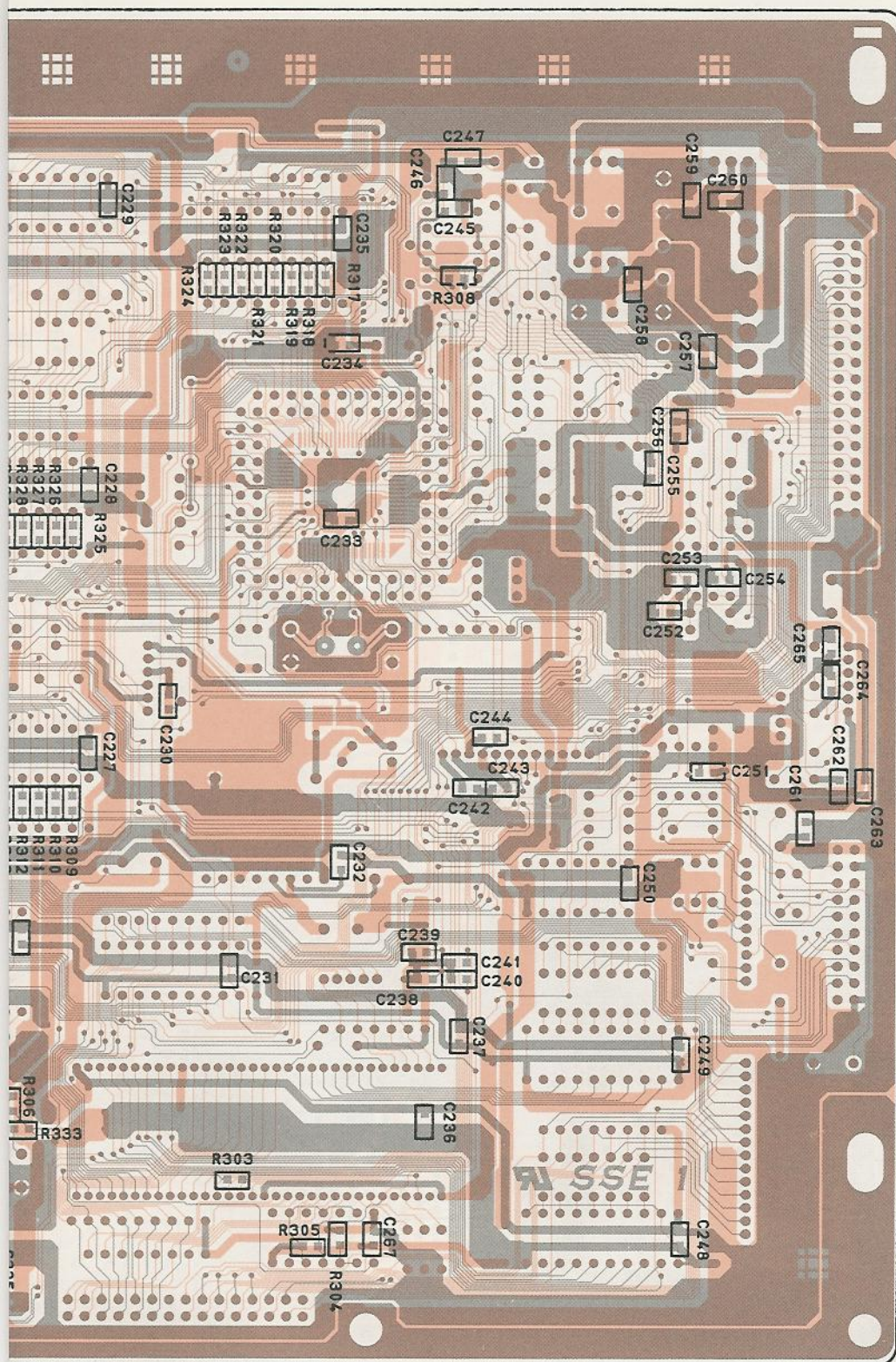
DM2 (VK287500) XJ555B0

1. IC
  - IC201: NJM4556 (IG042500) OP AMP.
  - IC202 ~ 205, 209 ~ 212, 214, 268, 269: M5238P R610 (XJ748A00) OP AMP.
  - IC206: YM3029 (XF237A00) DAC
  - IC207: NJM79L05 (IG130500) -5V REGULATOR
  - IC208: NJM78L05A (IG065510) +5V REGULATOR
  - IC213: PCM56P-Y (XH690A00) DAC
  - IC215, 216: YM7102 (XG996A00) PAN
  - IC217, 219: YM7103 (XG993A00) EGM2
  - IC218, 220: YM7107 (XG994A00) OPS3
  - IC221, 224: YM3807 (XA902001) MOD
  - IC222, 223: YM3422B (XE862B00) ESI
  - IC225: LC9116A-483 (XI364A00) TW80 DECODER
  - IC226, 227: YM6007 (XF164A00) DSP2
  - IC228: TMC57800N (XG662A00) MIX5
  - IC229 ~ 242: MB81464-12PSZ (XD265A00) DRAM 256K
  - IC243: M62021L (XH970A00) RESET
  - IC244 ~ 247: HM628128LP-10 (XI580A00) SRAM 1M
  - IC248: TC538200P-H100 (XI735B00) ROM 8M
  - IC249: MB838200-20P-G (XI734A00) ROM 8M
  - IC250: MB838200-20P-G (XI733A00) ROM 8M
  - IC251: MB838200-20P-G (XI732A00) ROM 8M
  - IC252: TC538200P-H099 (XI731B00) ROM 8M
  - IC253: LH538089 (XI730A00) ROM 8M
  - IC254: LH538088 (XI729A00) ROM 8M
  - IC255: LH538087 (XI728A00) ROM 8M
  - IC256, 257: YM7119 (XG995A00) M3
  - IC258 ~ 260: SN74ALS245ANSR (XE057A00) BUFFER
  - IC261, 264: SN74LS245ANSR (XH779A00) BUFFER
  - IC262, 263, 265: TC74HC245F-T1 (XD603A00) TRANSCEIVER
  - IC266: TC74HC00AF-TP1 (XD655A00) NAND
  - IC267: SN74HC74NSR (XC726001) DFF
  - IC270: TC74HC4051AF (XJ623A00) MULTIPLEXER
  - IC271, 272: SN74HC138NSR (XD835A00) DECODER
  - IC273: TC74HC21AF (XJ622A00) 2-4 IN AND
  - IC274: TC74HC175AF-TP1 (XD658A00) DFF
2. Transistor
  - Q201 ~ 208: 2SC2878 A, B (IC287820)
  - Q210: 2SA1115 E, F (IA111510)
3. Digital Transistor
  - Q209: DTC143XS TP (VD488500)
4. Diode
  - D202 ~ 204: 1SS133 (IF003450)
5. Resistor Array
  - RA201 ~ 203, 205 ~ 211: RGLD8X103J (VE445200)
  - RA204, 212, 213: RGLD4X103J (VE443500)
6. Trimmer Potentiometer
  - VR201: B100K EVN (VB593200)
7. Chip Resistor
  - R348 ~ 363: 100Ω 0.1W J (RD255100)
8. Semiconductive Cera. Cap.
  - C399 ~ 404: 0.1μ 25V Z (VC694800)
9. Chip Monolithic Cera. Cap.
  - C301 ~ 357, 359 ~ 388, 394 ~ 398: F 0.1μ 25V Z (VJ798800)
10. EMI Filter
  - EMI 201: LS MT Y223NB (FZ006970)
11. Quartz Crystal Unit
  - X201: AF2138CG (VI552000) 12.288MHz
12. Lithium Battery
  - B101: SONY/CR2032 (VE338400)







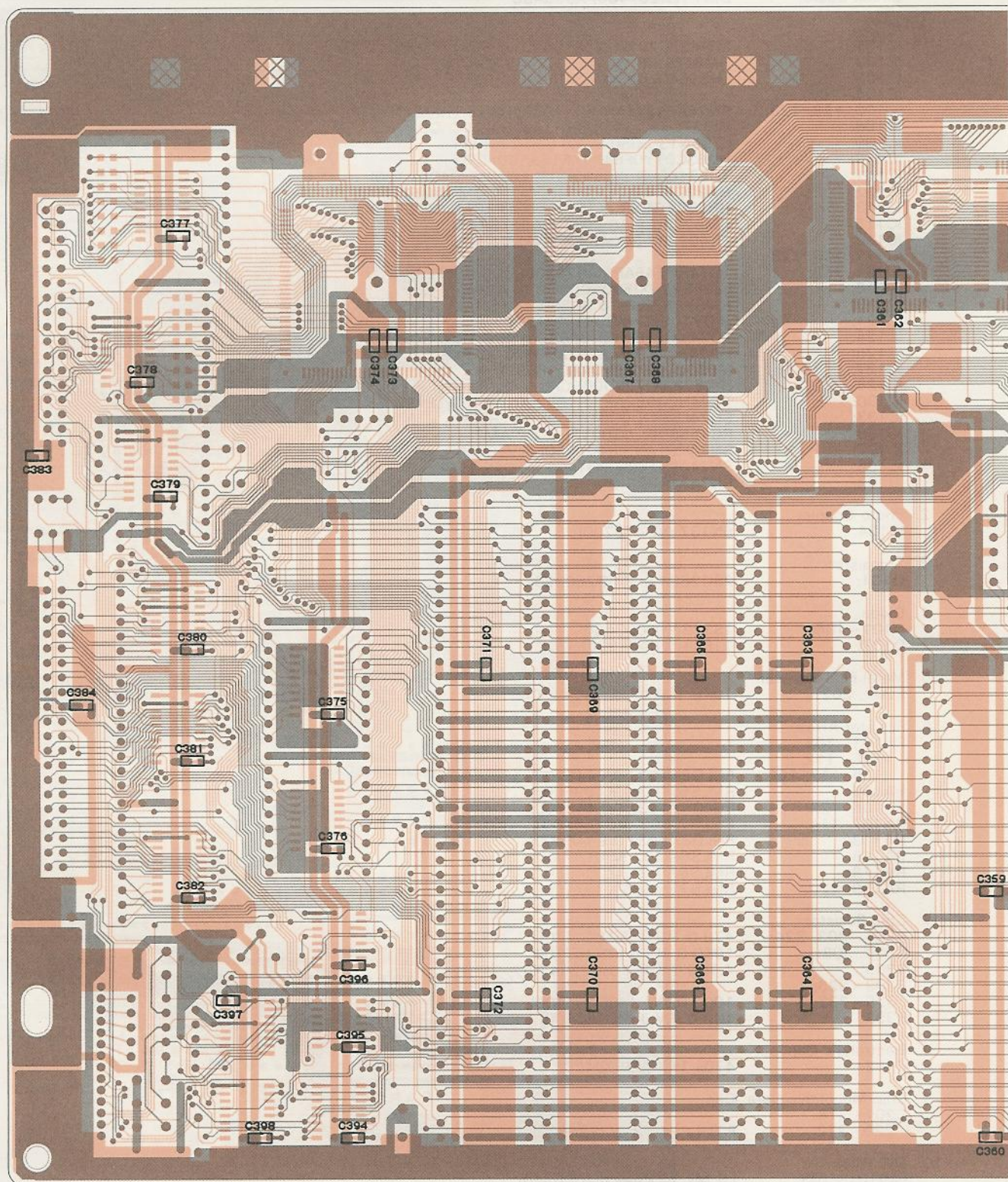


## Notes)

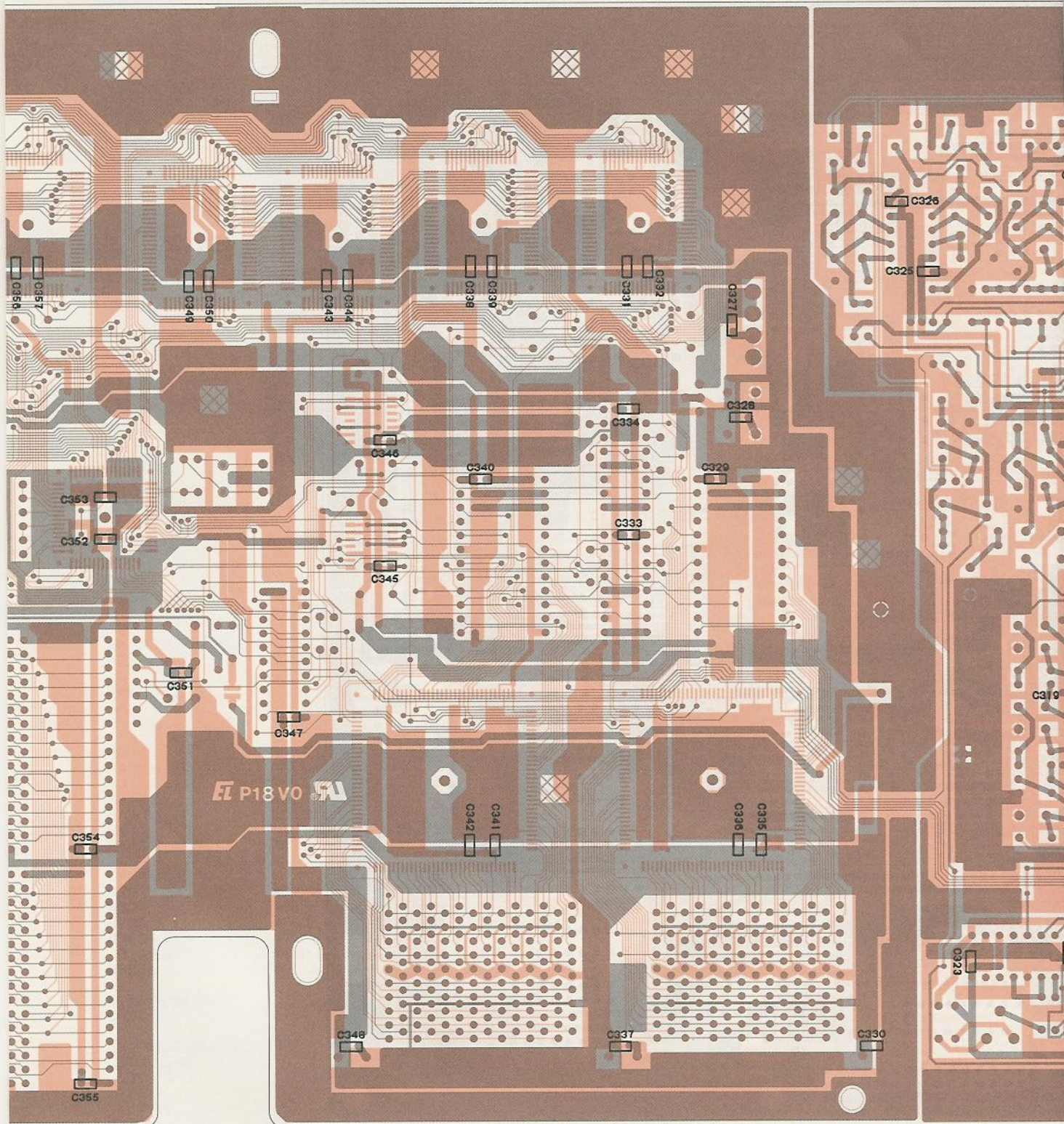
- Circuit Board: DM1 (VK287400) XJ55AB0
1. IC
    - IC101: M5M27C201K (XJ616C00) EPROM (040DV120)
    - IC102: HM658128P-12 (XE612A00) PSRAM
    - IC103: LH5164D-10L (XF876A00) SRAM
    - IC104 ~ 107, 122, 123, 129: SN74ALS245AN (IG149900) BUS TRANSCEIVER
    - IC108: WD37C65C-JM00 (XH129B00) FDD CONTROLLER
    - IC109: LZ95A13 (XI501A00) GATE ARRAY
    - IC110: HD63C01Y0F64P (XF148A00) CPU
    - IC111: TC574000D (XJ613D00) EPROM (040AV120)
    - IC112: HN27C101AG (XJ614B00) EPROM (040BV110)
    - IC113: HN27C101AG (XJ615C00) EPROM (040CV120)
    - IC115: HM62256LP-10 (XH266A00) SRAM
    - IC116: TC4093BP (IG043300) NAND
    - IC117, 120, 126, 131, 132: TC74HC245AP (IRO24500) BUS BUFFER
    - IC118: LZ95B12 (XI500A00) GATE ARRAY
    - IC119: HM628128LP-10 (XI580A00) SRAM
    - IC121:  $\mu$ PD71055C (XB361001) PPI
    - IC124: TC74AC245P (XH608A00) BUS TRANSCEIVER
    - IC125: HD63B01Y0RM21P (XG950C00) PKS
    - IC127: M62021L (XH970A00) RESET
    - IC128: H8/532 (XI722D00) CPU
    - IC130: TC74HC4052AP (IR405200) MULTIPLEXER
    - IC133: SN74LS14N (IG049650) INVERTER
    - IC135: RC4558D-V (IG001390) OP AMP.
    - IC137: SN74HC14N (IR001450) INVERTER
    - IC138: SN74ALS138N (IG149600) DECODER
    - IC139: SN74ALS32N (XA055001) OR
  2. Photo Coupler
    - IC134: 6N137 (VD473200)
  3. Transistor
    - Q101: 2SC2603 E, F (IC260320)
  4. Diode
    - D101 ~ 106: 1SS133 (IF003450)
    - D107: 11ES4 (VB481900)
  5. Metal Film Resistor
    - R201, 202: 10K $\Omega$  1/5W F (VA074400)
  6. Resistor Array
    - RA101 ~ 104, 108 ~ 112, 116, 117, 121: RGLD8X103J (VE445200)
    - RA105: RMLS5J102 (VK409500)
    - RA106, 122: RGLD4X103J (VE443500)
    - RA107, 114: RMLS7J103 (VG284400)
    - RA113: RGLD8X223J (VE445400)
    - RA115: RMLS6-223J (VA823000)
    - RA118: RMLS6J103 (HZ004650)
    - RA119, 120: RMLS7153J (VK437400)
  7. Chip Resistor
    - R301 ~ 303, 324: 47 $\Omega$  0.1W J (RD254470)
    - R304, 308: 10K $\Omega$  0.1W J (RD257100)
    - R305: 4.7K $\Omega$  0.1W J (RD256470)
    - R309 ~ 323, 325 ~ 332: 100 $\Omega$  0.1W J (RD255100)
    - R333: 1K $\Omega$  0.1W J (RD256100)
  8. Electrolytic Cap.
    - C102: 470 $\mu$  16V (UJ838470)
  9. Chip Monolithic Cera. Cap.
    - C201 ~ 218, 220 ~ 272: F 0.1 $\mu$  25V Z (VJ798800)
  10. EMI Filter
    - EMI101 ~ 103: LS MT Y223NB (FZ006970)
  11. Quartz Crystal Unit
    - CR101: 16MHz AT-49 (VI573400)
    - CR102: 12MHz AT-49 (VE463500)
    - CR103: 24MHz AT-49 (VK409400)
  12. Lithium Battery
    - B101: SONY/CR2032 (VE338400)



## ● DM2 Circuit Board (Pattern side — パターン側)







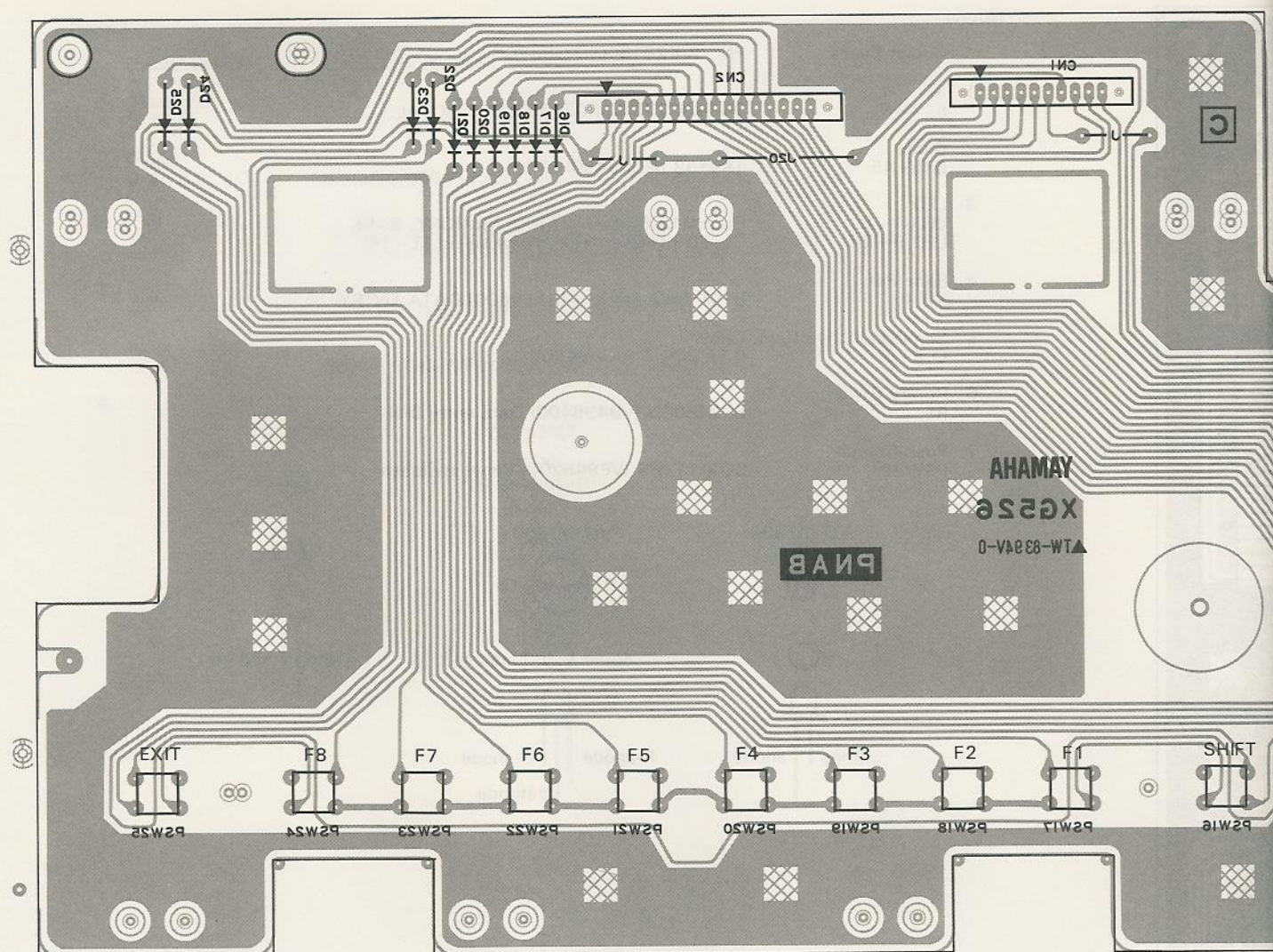


Circuit Board: DM2 (VK287500) XJ555B0

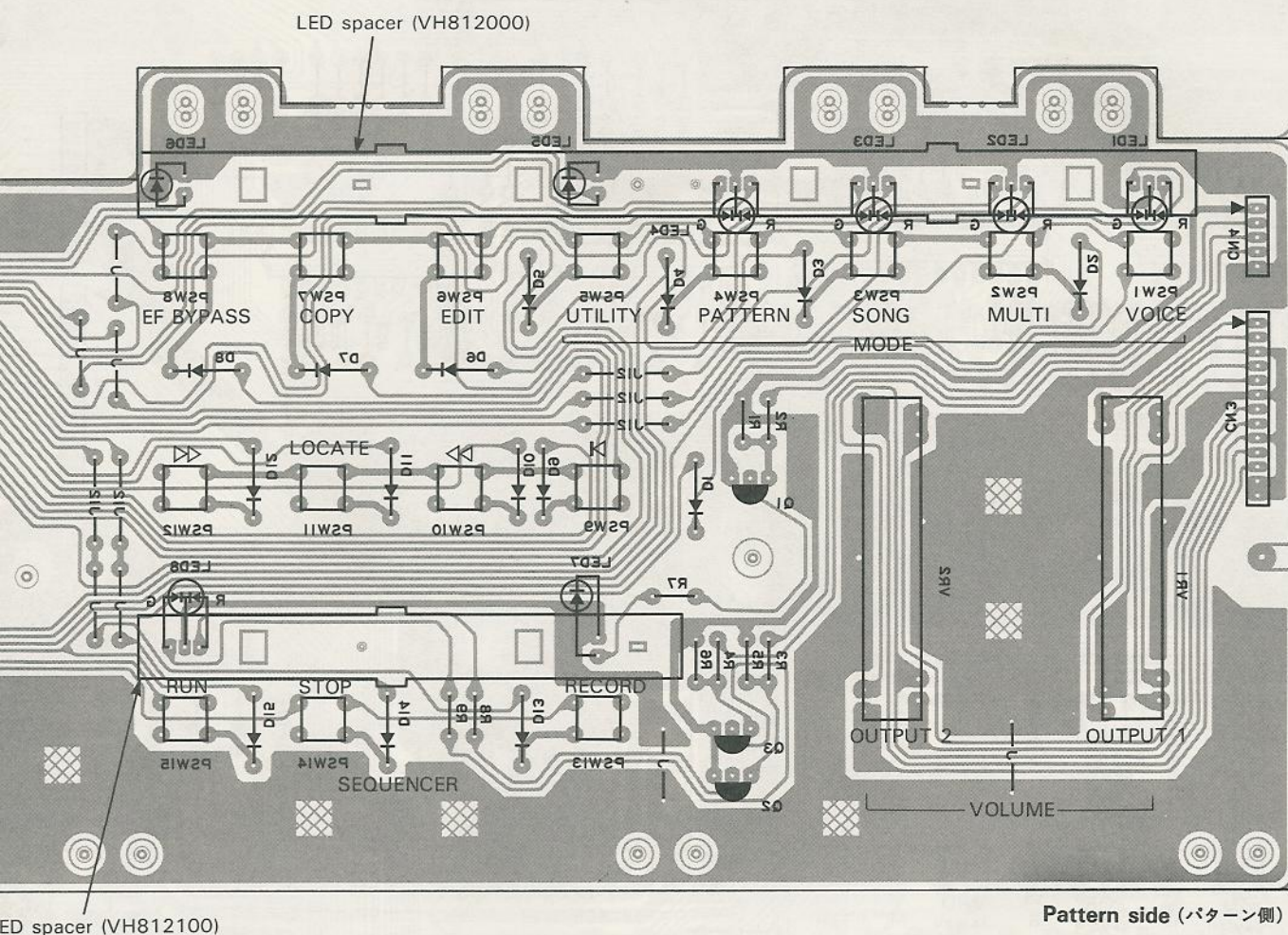
- 37-6



● PNAB Circuit Board

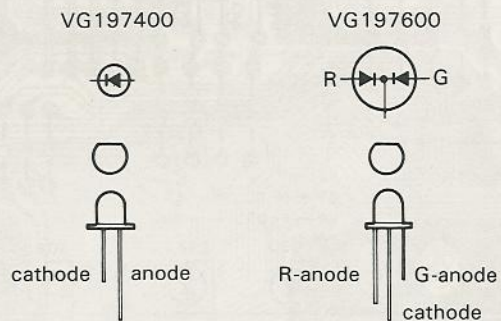




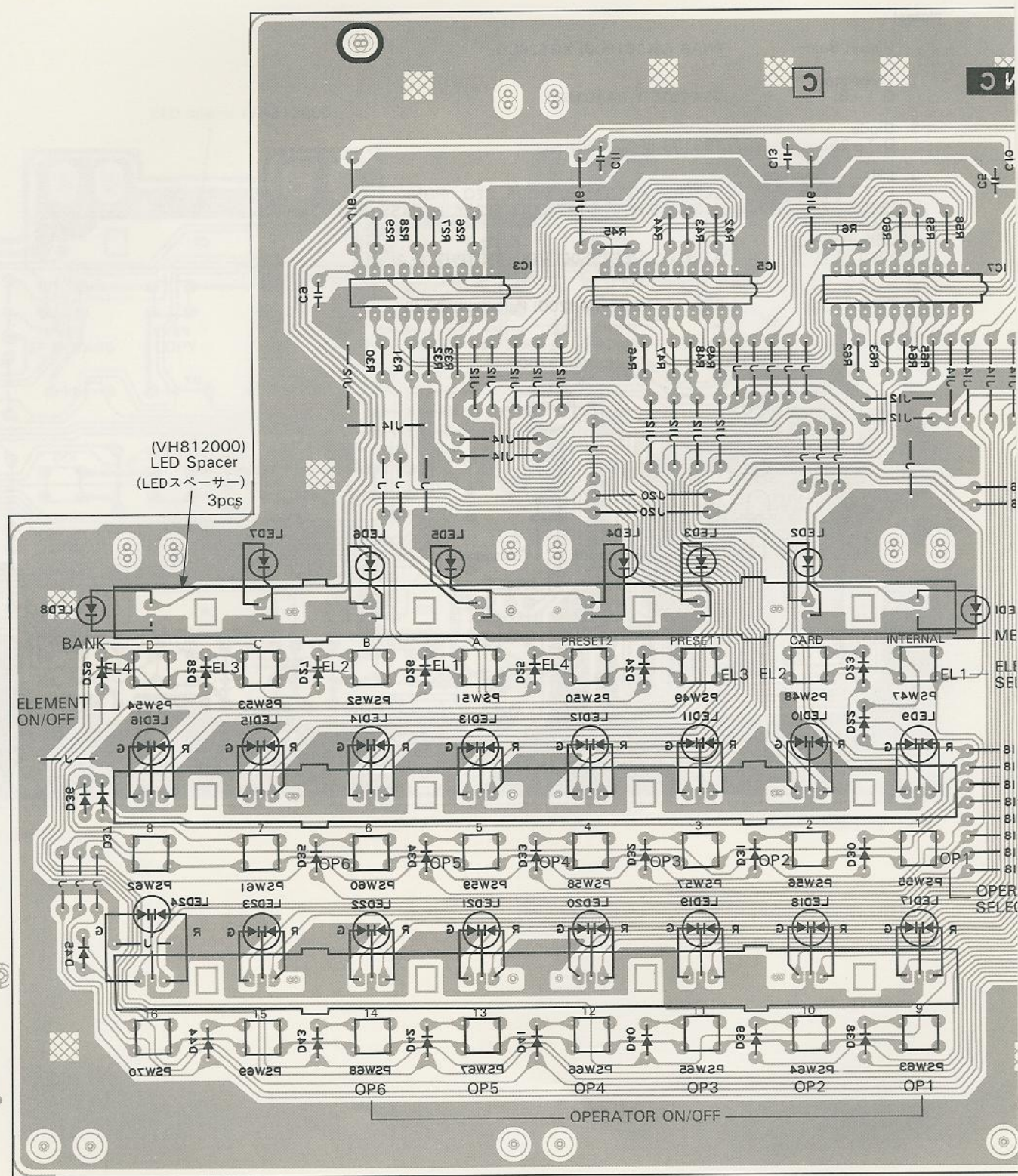


## Notes)

- Circuit Board: PNAB (VK261900) XG526C0
1. Transistor  
Q 1~3: 2SA1015 Y (IA101521)
  2. Diode  
D 1~25: 1SS133 (IF003450)
  3. LED  
LED 1~4, 8: GL3ED8 (VG197600) MODE, SEQ. (RUN)  
LED 5~7: GL3HD18 RE (VG197400) UTILITY, BYPASS, REC
  4. Slide Pot.  
VR 1, 2: A10K  $\times$  2 (VE373500) VOL. (OUTPUT 1, 2)
  5. Push Switch  
PSW 1~25: SOA-111HS (VF946200) Panel switches
  - 6.







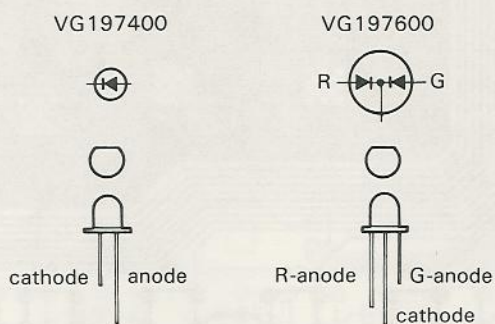




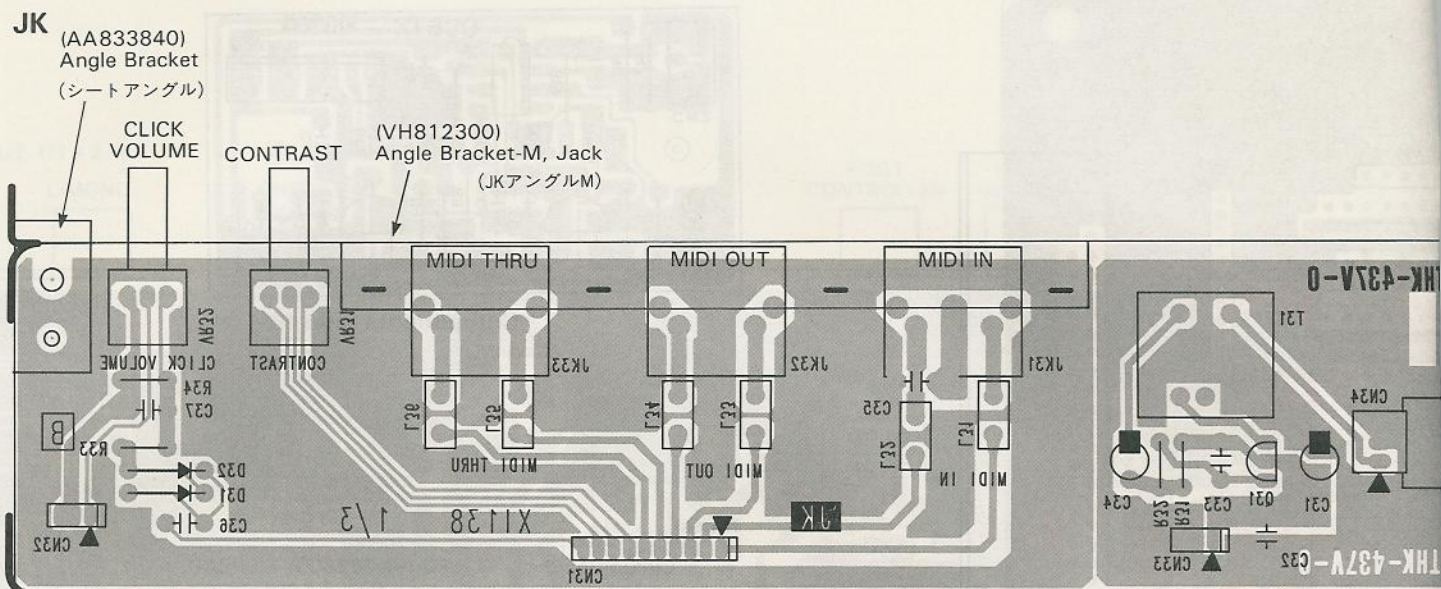


## Notes)

- Circuit Board: PNC (VK261800) XG527C0
1. IC  
IC 1 ~ 7: SN74HC273N (IR027350) DFF OCTAL
  2. Diode  
D 1 ~ 45: 1SS133 (IF003450)
  3. LED  
LED 1 ~ 8: GL3HD18 RE (VG197400) MEMORY, BANK  
LED 9 ~ 24: GL3ED8 (VG197600) Voice select (1 ~ 16)
  4. Slide Pot.  
VR 1: B10K EWA-NFOC (VC250600) DATA ENTRY
  5. Semiconductive Cera. Cap.  
C 2 ~ 5: 0.1 $\mu$  25V Z (VC694800)
  6. Rotary Switch  
RE: EC24B30D (VB436400) Data entry Dial
  7. Push Switch  
PSW26 ~ 70: SOA-111HS (VF946200) Panel switches
  - 8.



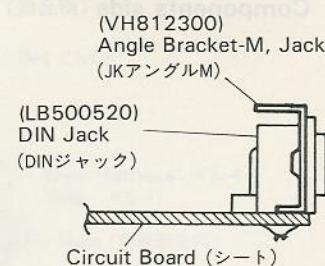
# ● JK Circuit Boards



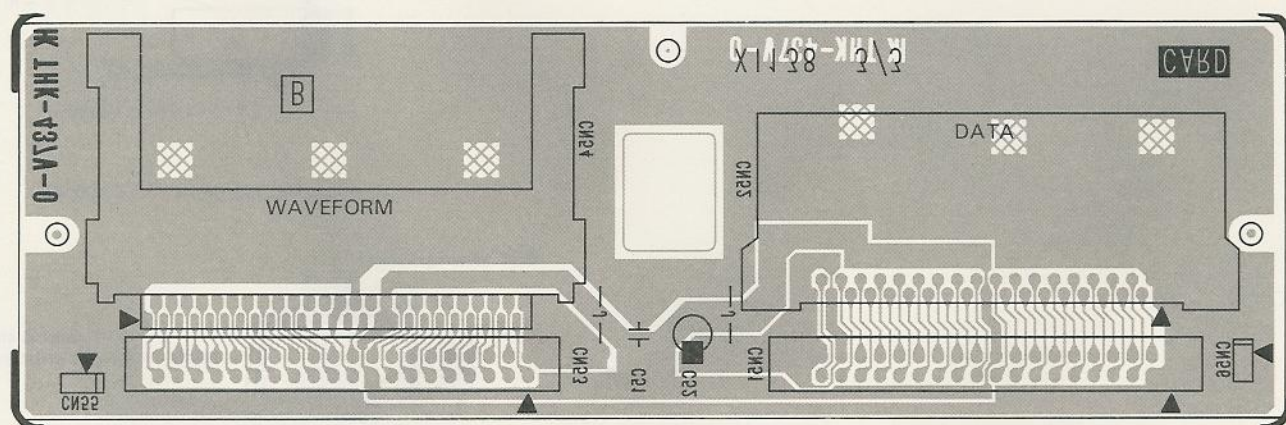
Pattern side (パターン側)

## Notes)

- |                               |                                    |             |            |                                    |
|-------------------------------|------------------------------------|-------------|------------|------------------------------------|
| Circuit Board:                | JK (JK) (NX809690) X1138D0         | 6. Coil     | L31 ~ 36:  | 20 $\mu$ H FL5R200QN (VB835000)    |
| 1. Transistor                 | 2SC945A PA (IC094530)              | 7. DIN Jack | JK31 ~ 33: | 5P TCS4650-01 (LB500520) MIDI (IN) |
| 2. Diode                      | 1SS133 (IF003450)                  |             |            |                                    |
| 3. Variable Resistor          | B1K EVU-E2A (VI573700) CONTRAST    |             |            |                                    |
| VR31:                         | A10K EVU-E (VD048800) CLICK VOLUME |             |            |                                    |
| VR32:                         |                                    |             |            |                                    |
| 4. Semiconductive Cera. Cap.  | 0.1 $\mu$ 25V Z (VC694800)         |             |            |                                    |
| C32, 35:                      |                                    |             |            |                                    |
| 5. DC/AC Inverter Transformer | D32-49A (VK458100)                 |             |            |                                    |
| T31:                          |                                    |             |            |                                    |



## CARD



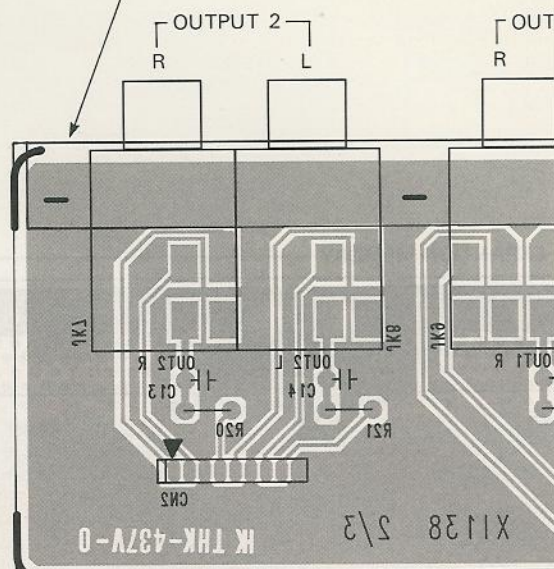
Pattern side (パターン側)

3NA1-VJ87540



JKB

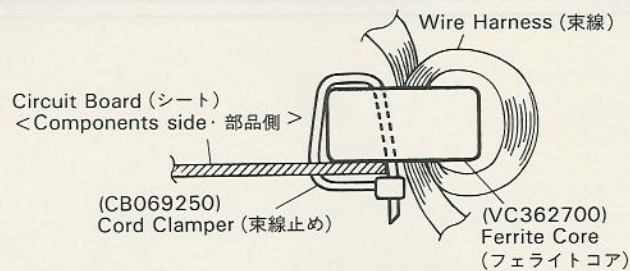
(VH812200)  
Angle Bracket-H, Jack  
(JKアングルH)



8. Ferrite Core  
FR31:

FR25/15/12-1400 (VC362700)

OUT, THRU)



## Notes)

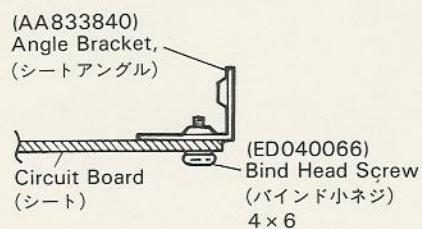
Circuit Board:

- Coil  
L 1~11:
- Phone Jack  
JK 1:  
JK 2, 3:  
JK 4, 5, 10:  
JK 6:  
JK 7, 8:  
JK 9:

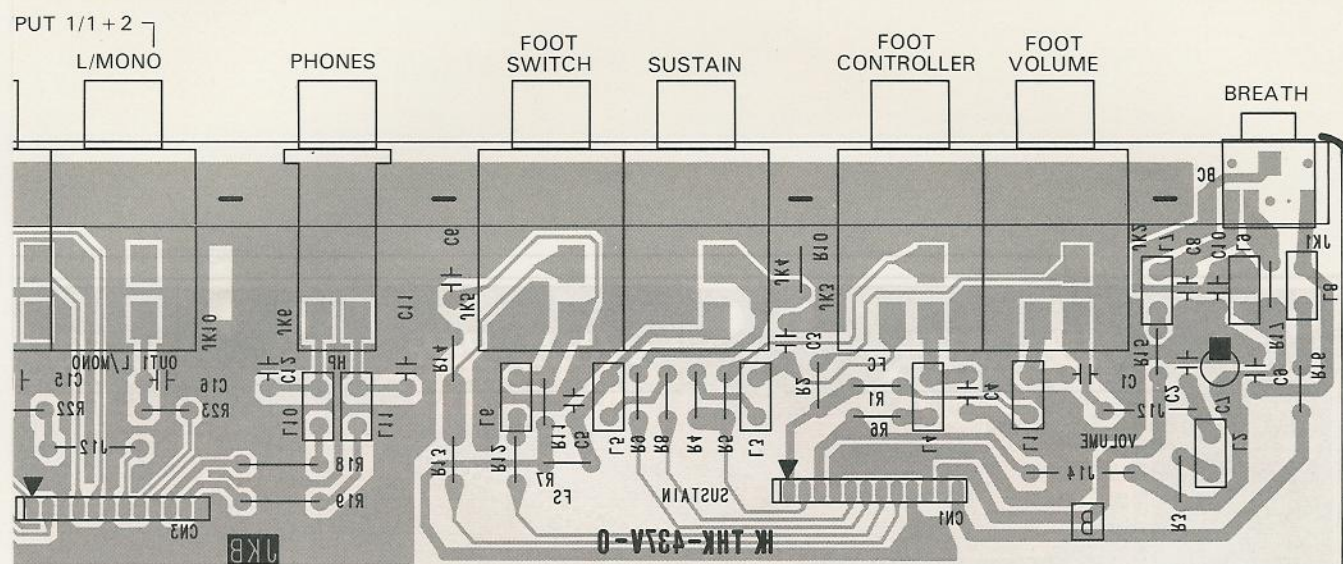
Notes)

Circuit Board: JK (CARD) (NX809710) X1138D0

- Semiconductive Cera. Cap.  
C51: 0.1 $\mu$  25V Z (VC694800)
- Connector, IC Card  
CN52: 38P IC3A-38PS-1.27D (VF821100) DATA  
CN54: 50P 264D-550P-28D8 (VH985300) WAVEFORM
- Angle Bracket, C.B.

Circ  
<C



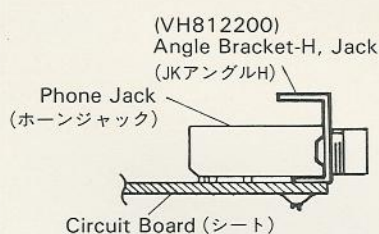


Pattern side (パターン側)

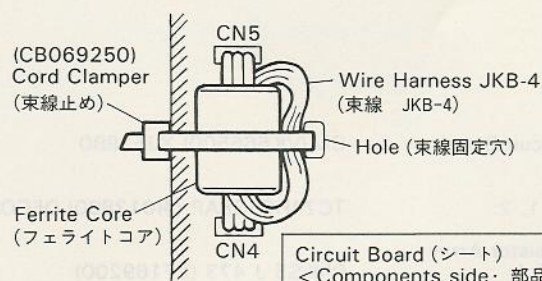
JK (JKB) (NX809700) XI138D0

20μH FL5R200QN (VB835000)

ST.MINI HSJ0912 (LB302010) BREATH  
 STEREO HLJ4306 (VE742200) F.VOLUME, F.CONT  
 MONO HLJ4306 (VE742000) SUS, F.SW, OUTP1 (L)  
 STEREO HLJ0521 (LB203090) PHONES  
 STEREO HLJ4306 (VI662400) OUTPUT 2 (L, R)  
 STEREO HLJ4306 (LB301780) OUTPUT 1/1+2 (R)

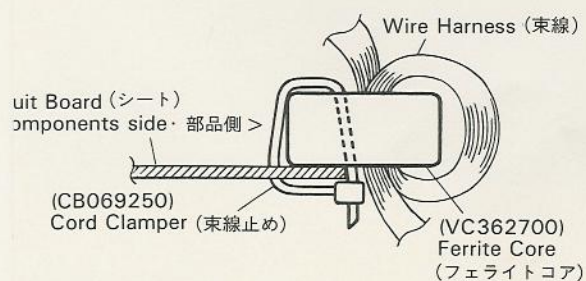


## 4. Connector Assembly JKB-4 (CN4-CN5)

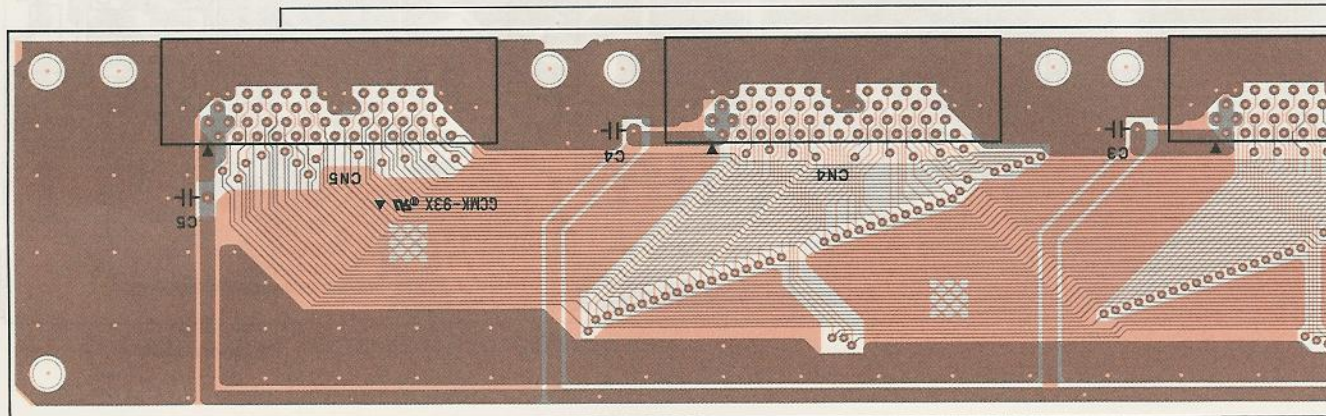


Circuit Board (シート)  
 <Components side・部品側>

FR25/15/12-1400 (VC362700)



● CN Circuit Board

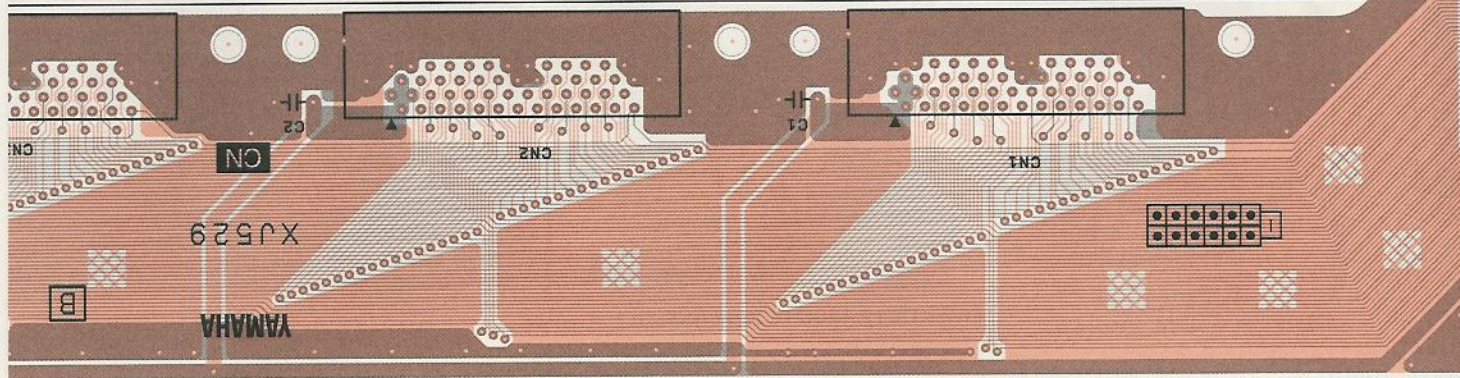


Notes)

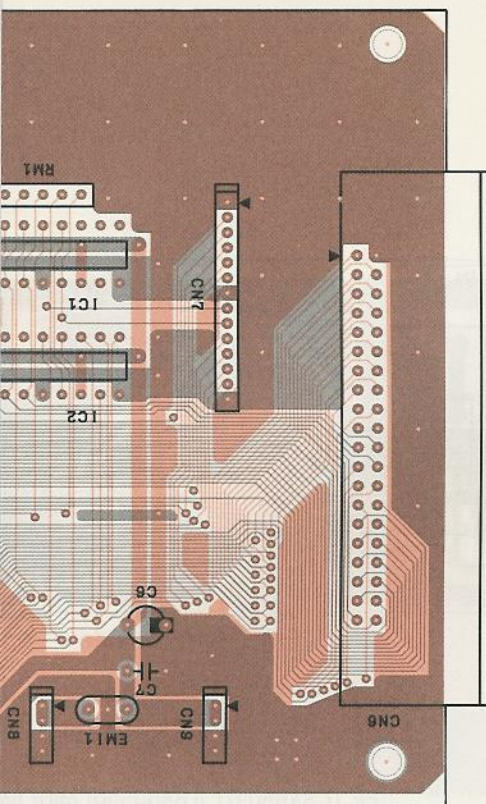
- |                              |                                  |
|------------------------------|----------------------------------|
| Circuit Board:               | CN (VK666500) XJ529B0            |
| 1. IC                        |                                  |
| IC 1, 2:                     | TC74HC138AP (IR013800) DECODER-8 |
| 2. Resistor Array            |                                  |
| RM 1:                        | RMLS5 J 473 (VF169200)           |
| 3. Semiconductive Cera. Cap. |                                  |
| C 1~5, 7, 8:                 | 0.1 $\mu$ 25V Z (VC694800)       |
| 4. EMI Filter                |                                  |
| EMI 1:                       | DSS306-93F223Z1 (VD542700)       |
| 5. Connector                 |                                  |
| CN 1~5:                      | FX2 52P SE (VL347400)            |
| CN 6:                        | HIF 40P SE (LB903400)            |



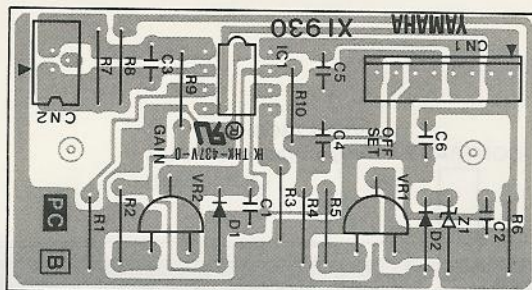
-EXPANTION MEMORY-



# ● PC Circuit Board



Components side (部品側)



Components side (部品側)

## Notes)

- |                          |                                   |
|--------------------------|-----------------------------------|
| Circuit Board:           | PC (VK263600) XI930A0             |
| 1. IC                    |                                   |
| IC 1:                    | RC4558D-V (IG001390) OP AMP.      |
| 2. Diode                 |                                   |
| D 1, 2:                  | 1SS176 (VA240700)                 |
| 3. Zener Diode           |                                   |
| Z 1:                     | 05AZ5.1Y 5.1V (VI692000)          |
| 4. Trimmer Potentiometer |                                   |
| VR 1:                    | B5K 3P EVN (HT370250) OFFSET ADJ. |
| VR 2:                    | B100K 3P EVN (HT370260) GAIN ADJ. |

CN: 3NA1-VK66650  
PC: 3NA1-VK26360



# ● PS Circuit Board

## Notes)

Circuit Board: PS (VJ800200) XI139C0 (J)  
PS (VJ800300) XI139C0 (U)  
PS (VJ800400) XI139C0 (C)  
PS (VJ800500) XI139C0 (H, D, A, B)

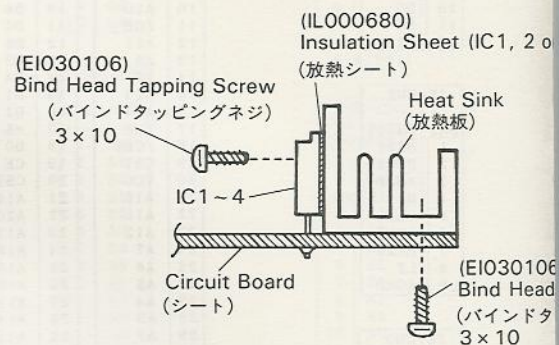
1. IC  
IC 1, 2: SI-3052V (IG136200) 5V 2A REGULATOR  
IC 3: AN78M12F (XD340001) +12V REGULATOR  
IC 4: AN79M12F (XD342001) -12V REGULATOR
2. Diode  
D 4~7: 11ES4 (VB481900)
3. Diode Stack  
D 1: D5FB20 5A 200V (IH001370)  
D 2: S4VB20 (IH001210) 2.6A 200V  
D 3: DF04M 1A 400V (VD488400)
4. Zener Diode  
Z 1, 2: MTZ6.8C 6.8V (IF010780)
5. Metal Oxide Film Resistor  
R 1: 220Ω 1W J (VC745800)
6. Ceramic Cap.  
C 1: 0.01μ 400V (FI494100)  
C 2, 3: 2200P 400V (FI383220)  
C 4, 5: 4700P 400V (FI383470) (H, D, A, B only)
7. Electrolytic Cap.  
C10, 11, 19: 10000μ 16V (UJ63A100)  
C27: 1000μ 25V (UJ649100)  
C29: 2200μ 25V (UJ649220)
8. Semiconductive Cera. Cap.  
C12, 13, 20, 21, 28, 30, 31, 33: 0.1μ 25V Z (VC694800)
9. Coil  
L 1: 3mH PLA3021A (GD900760)
10. Push Switch  
SW 1: ESB-8236V JUCS (VF576000) POWER
11. Fuse  
F 1 (J): T 5A 250V (KB000400)  
(U, C): T 5A 250V (KB002590)  
(H, D, A, B): T5A 250V S (KB000780)  
F 2 (U only): T 3A 250V (KB002650)  
F 3 (J): T 2.5A 250V (KB000420)  
(U, C): T 2.5A 250V (KB002680)  
(H, D, A, B): T2.5A 250V S (KB000690)

## 12. Jumper Wire & Fuse Label

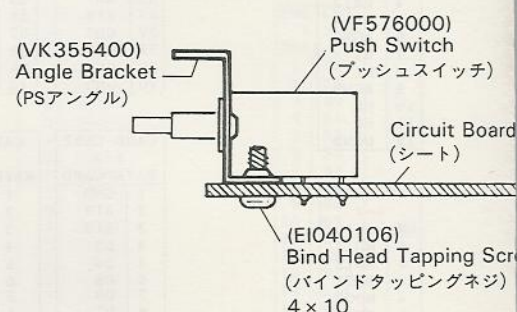
	J1	J2	Fuse Label
J	○	○	x
U	○	x	○
C	○	○	x
H, D, A, B	x	○	x

(○: installed x: not installed)

13.



14.

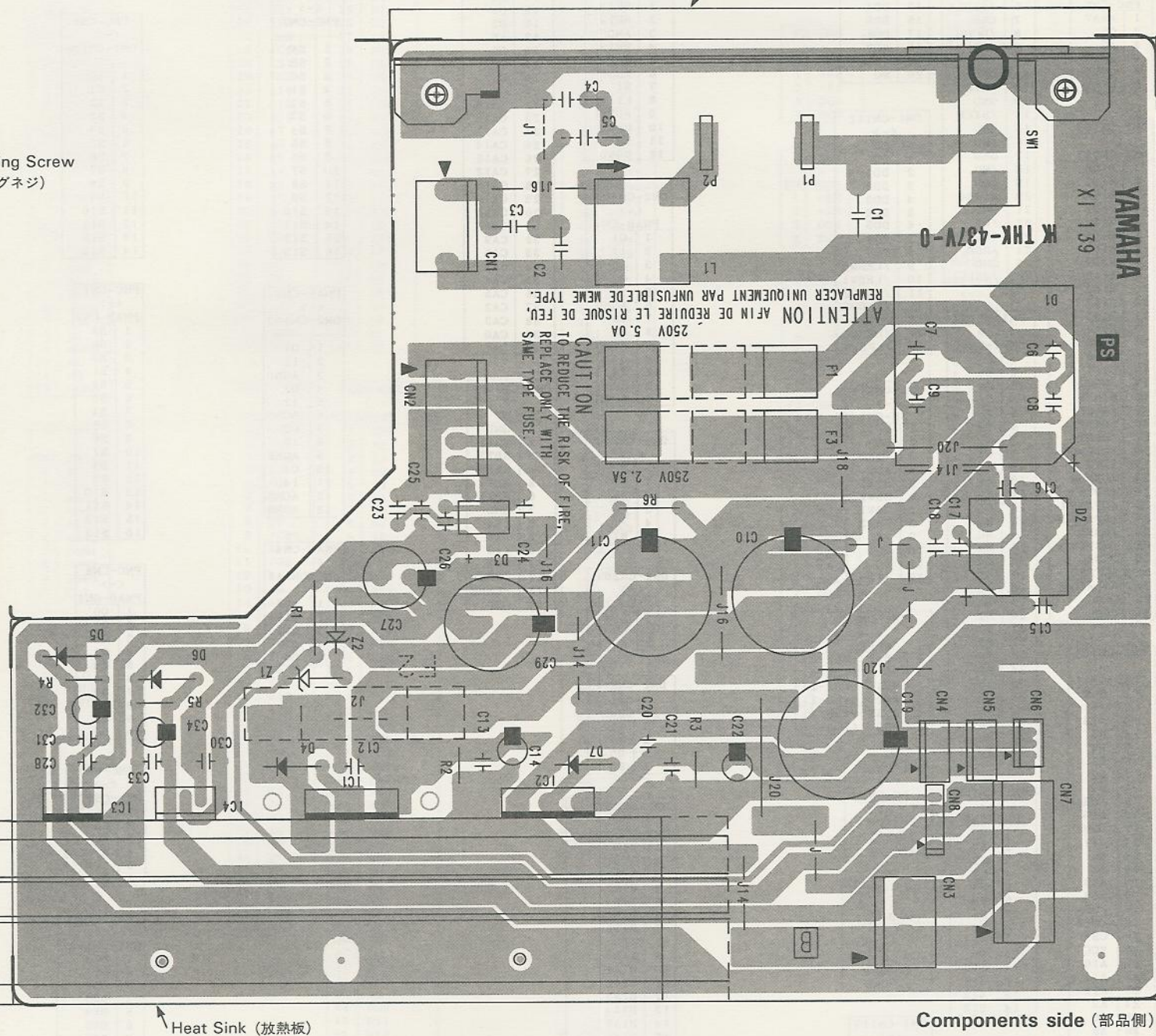




ly)

Tapping Screw  
（ネジ）

w

(VK355400)  
Angle Bracket, Power Sw.  
(PSアングル)

66AS



## • DM1

DM1-CN101 <->	
JK-CN31	
1	MDI1
2	MDI2
3	ND01
4	MD02
5	MDT1
6	MDT2
7	CON1
8	CON2
9	CON3
10	CLI

DM1-CN102 <->	
PNC-CN9	
1	+5AV
2	CS
3	AG
4	A
5	COM
6	B

DM1-CN103 <->	
DM2-CN207	
1	B1D0
2	B1D1
3	B1D2
4	B1D3
5	B1D4
6	B1D5
7	B1D6
8	B1D7
9	B1A0
10	B1A1
11	B1A2
12	B1A3
13	B1A4
14	B1A5
15	B1A6
16	B1A7
17	/RES2
18	B1R/W
19	/B1RD
20	/B1WR
21	/DDM2
22	/IRQM3
23	1BT2
24	/DEMG2
25	/DOPS3
26	/DPANFM
27	/DPANPCM
28	/M3FM
29	/M3PCM
30	FMSSEL
31	/CTS2
32	ANLATCH
33	GND
34	GND

DM1-CN104 <->	
CARD-CN51	
1	GND
2	A17
3	A18
4	D3
5	D4
6	D5
7	D6
8	D7
9	/CE1
10	A10
11	/OE
12	A11
13	A9
14	A8
15	A13
16	A14
17	/WE
18	/CE2
19	CST
20	VCC
21	A16
22	A15
23	A12
24	A7
25	A6
26	A5
27	A4
28	A3
29	A2
30	A1
31	A0
32	D0
33	D1
34	D2
35	MR
36	A19
37	CBT
38	GND
39	GND
40	GND

DM1-CN105 <->	
CN-CN9	
1	FD+5
2	FD+5
3	FDG
4	FDG

DM-CN106 <->	
FDD-CN	
1	+5V
2	/INDEX
3	+5
4	/DSELO
5	+5V
6	/DSEL1
7	GND
8	/DCHG
9	GND
10	/MTON
11	GND
12	/DIRC
13	GND
14	/STEP
15	GND
16	/WD
17	GND
18	/WG
19	GND
20	/TROO
21	GND
22	/WP
23	GND
24	/RDD
25	GND
26	/SSEL

DM1-CN107 <->	
MK2-CN1	
1	C#
2	D
3	D#
4	E
5	F
6	F#
7	G
8	G#
9	A
10	A#
11	B
12	C
13	NC
14	NC
15	M0
16	B0
17	M1
18	B1
19	M2
20	B2
21	M3
22	B3
23	M4
24	B4
25	M5
26	B5
27	M6
28	B6
29	NC
30	NC

DM1-CN108 <->	
PNC-CN6	
1	S0
2	S1
3	S2
4	S3
5	S4
6	S5
7	S6
8	S7
9	S8
10	S9
11	S10
12	S11
13	S12
14	S13

DM1-CN110 <->	
PNC-CN5	
1	SA
2	SB
3	SC
4	SD
5	SE

DM1-CN111 <->	
LCD-CN1	
1	FGND
2	GND
3	VDD1
4	VEE
5	NWR1
6	/B1RD
7	/LCD
8	B1A0
9	NC
10	/RES1
11	DD0
12	DD1
13	DD2
14	DD3
15	DD4
16	DD5
17	DD6
18	DD7
19	+5
20	NC

DM1-CN112 <->	
PNC-CN10	
1	DD0
2	DD1
3	DD2
4	DD3
5	DD4
6	DD5
7	DD6
8	DD7
9	/LEDW0
10	/LEDW1
11	/LEDW2
12	/LEDW3
13	/LEDW4
14	/LEDW5
15	/LEDW6

DM1-CN114 <->	
JK-CN1	
1	FVOL
2	FC
3	+5AD
4	ADG
5	SSW1
6	SSW2
7	FSW1
8	FSW2
9	+5
10	GND
11	BC
12	-12

DM1-CN115 <->	
WHEEL	
1	+5AD (VR3-3)
2	PB (VR1-2)
3	MW1 (VR2-2)
4	MW2 (VR3-2)
5	2.5V (VR3-4)
6	ADG (VR3-1)

DM1-CN116 <->	
PC-CN1	
1	AT
2	A00
3	+12
4	-12

DM1-CN117 <->	
PNAB-CN4	
1	+5
2	Q10
3	Q11
4	Q12
5	GND

DM1-CN119 <->	
PS-CN7	
1	+5AD
2	+5A
3	DGA
4	DGA
5	+12
6	ADG
7	-12

## • DM2

DM2-CN201 <->	
JK-CN2	
1	BR21
2	BR22
3	AGND
4	R2
5	BL21
6	AGND
7	BL22
8	L2
9	AGND

DM2-CN202 <->	
JK-CN3	
1	BR11
2	BR12
3	ANG
4	BR13
5	BR14
6	AGND
7	R1
8	L1
9	AGND
10	HL
11	HR
12	HGND

DM2-CN203 <->	
PNAB-CN3	
1	O1
2	I1
3	AGND
4	O2
5	I2
6	AGND
7	O3
8	I3
9	AGND
10	O4
11	I4
12	AGND
13	AGND

DM2-CN204 <->	
PS-CN8	
1	+12
2	AG
3	AG
4	-12
5	MT

DM2-CN205 <->	
JK-CN32	
1	CI.I
2	NC
3	AGND

DM2-CN206 <->	
PS-CN3	
1	+5
2	+5
3	DG
4	DG

DM2-CN207 <->	
DM1-CN103	
1	B1D0
2	B1D1
3	B1D2
4	B1D3
5	B1D4
6	B1D5
7	B1D6
8	B1D7
9	B1A0
10	B1A1
11	B1A2
12	B1A3
13	B1A4
14	B1A5
15	B1A6
16	B1A7
17	/RES2
18	B1R/W
19	/B1RD
20	/B1WR
21	/DDM2
22	/IRQM3
23	1BT2
24	/DEMG2
25	/DOPS3
26	/DPANFM
27	/DPANPCM
28	/M3FM
29	/M3PCM
30	FMSSEL
31	/CTS2
32	ANLATCH
33	GND
34	GND

## • PNAB

PNAB-CN1 <->	
PNC-CN8	
1	Q0
2	Q1
3	Q2
4	Q3
5	Q4
6	Q5
7	Q6
8	Q7
9	Q8
10	Q9

PNAB-CN2 <->	
PNC-CN7	
1	SA
2	SB
3	S0
4	S1
5	S2
6	S3
7	S4
8	S5
9	S6
10	S7
11	S8
12	S9
13	S10
14	S11
15	S12
16	S13

PNAB-CN3 <->	
DM2-CN203	
1	O1
2	I1
3	AGND
4	O2
5	I2
6	AGND
7	O3
8	I3
9	AGND
10	O4
11	I4
12	AGND
13	AGND

PNAB-CN4 <->	
DM1-CN117	
1	+5V
2	Q10
3	Q11
4	Q12
5	DG

## • PNC

PNC-CN5 <->	
DM1-CN110	
1	SA
2	SB
3	SC
4	SD
5	SE
6	+5V
7	-
8	DG
9	-

(1-5:DM1)  
(6-9:PS1)

PNC-CN6 <->	
DM1-CN108	
1	S0
2	S1
3	S2
4	S3
5	S4
6	S5
7	S6
8	S7
9	S8
10	S9
11	S10
12	S11
13	S12
14	S13

PNC-CN7 <->	
PNAB-CN2	
1	SA
2	SB
3	S0
4	S1
5	S2
6	S3
7	S4
8	S5
9	S6
10	S7
11	S8
12	S9
13	S10
14	S11
15	S12
16	S13

PNC-CN8 <->	
PNAB-CN1	
1	Q0
2	Q1
3	Q2
4	Q3
5	Q4
6	Q5
7	Q6
8	Q7
9	Q8
10	Q9

PNC-CN9 <->	
DM1-CN102	
1	+5AV
2	CS
3	AG
4	A
5	COM
6	B

PNC-CN10 <->	
DM1-CN112	
1	DD0
2	DD1
3	DD2
4	DD3
5	DD4
6	DD5
7	DD6
8	DD7
9	/LEDW0
10	/LEDW1
11	/LEDW2
12	/LEDW3
13	/LEDW4
14	/LEDW5
15	/LEDW6



## • JK

JK-CN1 <->	
DM1-CN114	
1	FVL
2	FC
3	+5AD
4	AG
5	SSW1
6	SSW2
7	FSW1
8	FSW2
9	+5
10	DG
11	BC
12	-12

JK-CN2 <->	
DM2-CN201	
1	BR21
2	BR22
3	AGND
4	R2
5	BL21
6	AGND
7	BL22
8	L2
9	AGND

JK-CN3 <->	
DM2-CN202	
1	BR11
2	BR12
3	ANG
4	BR13
5	BR14
6	AGND
7	R1
8	L1
9	AGND
10	HL
11	HR
12	HGND

JK-CN31 <->	
DM1-CN101	
1	MD11
2	MD12
3	MDO1
4	MDO2
5	MDT1
6	MDT2
7	CON1
8	CON2
9	CON3
10	CL1

JK-CN32 <->	
DM2-CN205	
1	CLO
2	AGND
3	AGND

JK-CN33 <->	
PS-CN6	
1	+5
2	GND
3	GND

JK-CN34 <->	
LCD	
1	AC
2	GND
3	GND

## • CARD

CARD-CN51 <->	
DM1-CN104	
1	GND
2	A17
3	A18
4	D3
5	D4
6	D5
7	D6
8	D7
9	/CE1
10	A10
11	/OE
12	A11
13	A9
14	A8
15	A13
16	A14
17	/WE
18	/CE2
19	CST
20	VCC
21	A16
22	A15
23	A12
24	A7
25	A6
26	A5
27	A4
28	A3
29	A2
30	A1
31	A0
32	D0
33	D1
34	D2
35	MR
36	A19
37	CBT
38	GND
39	GND
40	GND

CARD-CN52 <->	
DATA CARD	
1	GND
2	A17
3	A18
4	D3
5	D4
6	D5
7	D6
8	D7
9	/CE1
10	A10
11	/OE
12	A11
13	A9
14	A8
15	A13
16	A14
17	/WE
18	/CE2
19	CST
20	VCC
21	A16
22	A15
23	A12
24	A7
25	A6
26	A5
27	A4
28	A3
29	A2
30	A1
31	A0
32	D0
33	D1
34	D2
35	MR
36	A19
37	CBT
38	GND

CARD-CN53 <->	
DM2-CN208	
1	D15
2	GND
3	D13
4	D14
5	D11
6	D12
7	D9
8	D10
9	D7
10	D8
11	D5
12	D6
13	D3
14	D4
15	D1
16	D2
17	+5
18	D0
19	CE
20	CST
21	A19
22	A20
23	A17
24	A18
25	A15
26	A16
27	A13
28	A14
29	A11
30	A12
31	A9
32	A10
33	A7
34	A8
35	A5
36	A6
37	A3
38	A4
39	A1
40	A2

CARD-CN54 <->	
WAVEFORM CARD	
1	GND
2	A1
3	A2
4	A3
5	A4
6	A5
7	A6
8	A7
9	A8
10	A9
11	A10
12	A11
13	A12
14	A13
15	A14
16	A15
17	A16
18	A17
19	A18
20	A19
21	A20
22	NC
23	/WE
24	/RAM/ROM
25	CE1
26	CE2
27	/WPROT
28	/OE
29	CST
30	VBB
31	VCC
32	VCC
33	VPP
34	D0
35	D1
36	D2
37	D3
38	D4
39	D5
40	D6
41	D7
42	D8
43	D9
44	D10
45	D11
46	D12
47	D13
48	D14
49	D15
50	GND

## • CN

CN-CN6 <->	
CARD-CN53	
DM2-CN208	
1	D15
2	GND
3	D13
4	D14
5	D11
6	D12
7	D9
8	D10
9	D7
10	D8
11	D5
12	D6
13	D3
14	D4
15	D1
16	D2
17	+5
18	D0
19	CE
20	CST
21	CA18
22	CA19
23	CA16
24	CA17
25	CA14
26	CA15
27	CA12
28	CA13
29	CA10
30	CA11
31	CA8
32	CA9
33	CA6
34	CA7
35	CA4
36	CA5
37	CA2
38	CA3
39	CA0
40	CA1

CN-CN7 <->	
DM2-CN209	
1	GND
2	SBT1
3	SBT2
4	SBT3
5	SBT4
6	SBT5
7	GND
8	/Y4
9	/Y5
10	/IC
11	/OE
12	/MSBW
13	/LSBW
14	GND

CN-CN8 <->	
PS-CN5	
1	+5B
2	+5B
3	DGB
4	DGB

CN-CN9 <->	
DM1-CN105	
1	FD+5
2	FD+5
3	FDG
4	FDG

## • PC

PC-CN1 <->	
DM1-CN116	
1	-12
2	-12
3	+12
4	+12
5	E
6	E
7	SO
8	E

## • PS

PS-CN1 <->	
P.T.	
1	AC1
2	NC
3	NC
4	AC2

PS-CN2 <->	
P.T.	
1	+A1
2	+A2
3	+B1
4	AE
5	+B2

PS-CN3 <->	
DM2-CN206	
1	+5A
2	+5A
3	DGA
4	DGA

PS-CN4 <->	
PNC-CN5	
1	+5B
2	+5B
3	DGB
4	DGB

PS-CN5 <->	
CN-CN8	
1	+5B
2	+5B
3	DGB
4	DGB

PS-CN6 <->	
JK-CN3	
1	+5B
2	DGB
3	DGB

PS-CN7 <->	
DM1-CN119	
1	+5AD
2	+5AD
3	DGA
4	DGA
5	+12
6	ADG
7	-12

PS-CN8 <->	
DM2-CN204	
1	+12
2	AG
3	AG
4	-12
5	MT

## • MK1

MK1-CN1 <->	
MK2-CN1	
1	C#
2	D
3	D#
4	E
5	F
6	F#
7	G
8	G#
9	A
10	A#
11	B
12	C
13	NC
14	NC
15	M0
16	B0
17	M1
18	B1
19	M2
20	B2

## • MK2

MK2-CN1 <->	
MK1-CN1	
1	C#
2	D
3	D#
4	E
5	F
6	F#
7	G
8	G#
9	A
10	A#
11	B
12	C
13	NC
14	NC
15	M0
16	B0
17	M1
18	B1
19	M2
20	B2
21	M3
22	B3
23	M4
24	B4
25	M5
26	B5
27	M6
28	B6
29	NC
30	NC



## ■ TEST PROGRAM

### VERSION DISPLAY MODE

In order to verify the ROM versions of the SY99, you may want to initiate the Version Display Mode. To initiate this mode press and hold the [Voice], the [INTERNAL], and the [1] switches then the versions of the MAIN ROM and SEQUENCE (SEQ) ROM will be displayed. Press [EXIT] to return to the main program.

### A. HOW TO ENTER THE TEST PROGRAM

Turn on the power switch of the SY99 and wait until the LCD has initialized and displays a normal operating mode message. While pressing the [VOICE] switch, press and hold the [BANK D] switch then the [8] switch. The SY99 will run the INITIAL TEST routine (refer to the INITIAL TEST section for details) and indicate that you have entered the Test Program by displaying the following message.

```
*** SY99 TEST Ver #.## *** Please Select

Main ROM : Version #.## 1990-10-??
SEQ. ROM : Version #.## 1990-10-??

[-1] : AUTO           [+1] : MANUAL

[ COPY ] : Fact.set   [EXIT] : Exit
```

Use the [-1], [+1], [COPY], or [EXIT] panel switches to select the appropriate test mode. If you press [-1], the auto test mode will be initiated. If you press [+1], the MANUAL test mode will be initiated. If you press [COPY], the SY99 will execute Test 49, "49. Factory settings", and then automatically exit the test mode and return to play mode (refer to Test 49 for details).

If you press [EXIT], you will exit the test mode and return to the play mode. The MANUAL mode is the preferred method of running the test program because it allows you to select or jump to any test and execute it. AUTO mode automatically executes each test in a fixed order. Some of the tests in the AUTO mode are automatically executed due to the nature of the test. In the AUTO mode simply press the [+1] switch to exit and automatically execute the next test or press [EXIT] to abort the test, then press [+1] to automatically execute the next test.

### B. PROCEEDING THROUGH THE TESTS

(\*\*MOST OF THESE FUNCTIONS MAINLY PERTAIN TO THE MANUAL TEST MODE\*\*)

When you enter the test program, the following display will appear.

```
*** SY99 TEST Ver #.## *** MODE : MANUAL

* 01 : ROM CHECK
  02 : RAM Read/Write
  03 : SEQUENCER ROM
  04 : SEQUENCER RAM
  05 : RAM Battery
```

Use the [+1], [-1], [ENTER], [COPY], [PAGE+], [PAGE-], [EXIT], or the numeric key pad, or the rotary encoder to move through the various tests of the test program.

Pressing: [+1] will execute the test which follows the current test.

[-1] will execute the test which precedes the current test.

[ENTER] will execute the currently selected test.

[PAGE+] will select the test which follows the current test and displays the test items.

[PAGE-] will select the test which precedes the current test and displays the test items.

[EXIT] will execute Test 50, "50. EXIT" (refer to Test 50 for details).

The numeric keys 0 through 9 of the entry pad can be used to enter a two-digit number to directly select a test. Simply enter the number and then press the [ENTER] switch. For example, if you would like to select TEST 6, press [0], [6] then press the [ENTER] switch.

**TEST SELECTION WHEN AN ERROR IS DETECTED**

In each of the following tests listed below, if an NG (No Good) error is detected, the following operations of the test will make the SY99 wait for the entry of a test number. You can then retry the test or perform another test. If you press [EXIT], the SY99 will wait for the entry of a test number.

- |                        |                         |                        |
|------------------------|-------------------------|------------------------|
| 9. Panel switches      | 10. Pitch bend          | 11. Modulation wheel 1 |
| 12. Modulation wheel 2 | 13. Data entry          | 14. Rotary encoder     |
| 15. Keyboard           | 16. Aftertouch          | 17. MIDI IN/OUT/THRU   |
| 18. Card insert        | 20. Card protect switch | 22. Wave card insert   |
| 26. Disk eject         | 27. Breath controller   | 28. Foot volume        |
| 29. Foot controller    | 30. Sustain switch      | 31. Foot switch        |
| 48. Jacks all off      |                         |                        |

**INITIAL TEST**

The following tests will be performed automatically when the test program is initiated.

- A. Read/write check for the RAM work area of CPU (IC128) of the DM1 circuit board.
- B. Checks the interrupt levels of both M3 ICs (IC256 & IC257) of the DM2 circuit board.

**DISPLAY OF TEST RESULTS**

If each test checks OK then the Test program proceeds to the Test Program entry display.  
If Test A is NG the RAM WORK AREA may be at fault and the display will indicate:

\*\* IC128(RAM) ERROR, TEST CONTINUE? \*\*

If Test B is NG then the error may be related to one of the M3 IC's IRQ levels.  
The display will indicate the error by showing the following message:

\* M3 IRQ CHECK ERROR, TEST CONTINUE? \*

**EXITING THE TEST**

This test automatically proceeds to the Test Program entry display if the items under test are OK.  
If an error message occurs press [YES] to exit the test.  
However, a RAM ERROR may not allow the SY99 to function normally.

**TEST PROGRAM TEST 1 – 50 (MANUAL MODE OPERATION)****1. TEST 1: SYSTEM ROM TEST**

\* 01; ROM CHECK

Performs a read test on the ROM for the following addresses.

IC111 : 80000h – 800Fh	IC111 : A0000h – A00Fh
IC111 : C0000h – C00Fh	IC111 : E0000h – E00Fh
IC112 : 60000h – 600Fh	IC113 : 10000h – 100Fh

(This test checks only 16 bytes.)

**DISPLAY OF TEST RESULTS**

OK

\* 01: ROM CHECK

OK

or

NG

\* 01: ROM CHECK

n:ICxxx

NG

(where n = ROM # and xxx = IC #)

**TEST END**

Ends after displaying the results.

**2. TEST 2: SYSTEM RAM TEST**

* 02: RAM Read/Write
----------------------

Performs a read/write test of RAM on the following addresses.

IC119 : 4000h – 5FFFh

IC115 : 3000h – 37FFFh

**DISPLAY OF TEST RESULTS**

OK	* 02: RAM Read/Write	OK
----	----------------------	----

or

NG	* 02: RAM Read/Write IC119	NG
----	----------------------------	----

**TEST END**

Ends after displaying the results. All RAM data is preserved.

**3. TEST 3: SEQUENCER ROM TEST**

* 03: SEQUENCER ROM
---------------------

Performs a read test on the ROM (IC101) of DM1 circuit board.

IC101 : 8000h – BFFFh 7 banks (#0 – #6)

C000h – FFFFh 1 bank (#7)

**DISPLAY OF TEST RESULTS**

OK	* 03: SEQUENCER ROM	OK
----	---------------------	----

NG	* 03: SEQUENCER ROM	NG
----	---------------------	----

**TEST END**

Ends after displaying the results.

**4. TEST 4: SEQUENCER RAM TEST**

* 04: SEQUENCER RAM
---------------------

Performs a RAM read/write test on all addresses of IC103 (RAM 1), IC102 (RAM 2).

1. IC103 : 4000h – 5FFFh

2. IC102 : 6000h (WINDOW 0), 6200h (WINDOW 1), 6400h (WINDOW 2), 6600h (WINDOW 3)

**DISPLAY OF TEST RESULTS**

OK	* 04: SEQUENCER RAM	OK
----	---------------------	----

NG	* 04: SEQUENCER RAM ICxxx	NG
----	---------------------------	----

(xxx = IC #)

**TEST END**

Ends after displaying the results. All RAM data is preserved.

5. TEST 5: RAM BACKUP BATTERY TEST

\* 05: RAM Battery

This test checks that the voltage of the RAM backup battery is greater than 2.9V and less than 3.3V.

DISPLAY OF TEST RESULTS

OK	* 05: RAM Battery	3.2V	OK
NG	* 05: RAM Battery	#. #V Low	NG
	* 05: RAM Battery	#. #V High	NG

TEST END

Ends after displaying the test results.

6. TEST 6: LCD – ALL DOTS “ON” TEST

\* 06: LCD All On

Check that all dots of the LCD change to black (ON) and contrast of the LCD can be controlled by the contrast volume.

DISPLAY OF TEST RESULTS

First, the display indicates “\* 06 LCD All On”, then all dots of the LCD change to black (ON).

TEST END

Press [EXIT] to end the test. The display shown below will appear and the SY99 will wait for you to enter a test number.

\* 06: LCD All On

7. TEST 7: LCD – ALL DOTS “OFF” TEST

\* 07: LCD All Off

Check that all dots change to white (OFF).

DISPLAY OF TEST RESULTS

First, the display indicates “\* 07 LCD All OFF”, then all dots of the LCD change to white (OFF).

TEST END

Press [EXIT] to end the test. The display shown below will appear and the SY99 will wait for you to enter a test number.

\* 07: LCD All Off

8. TEST 8: LED ON/OFF TEST

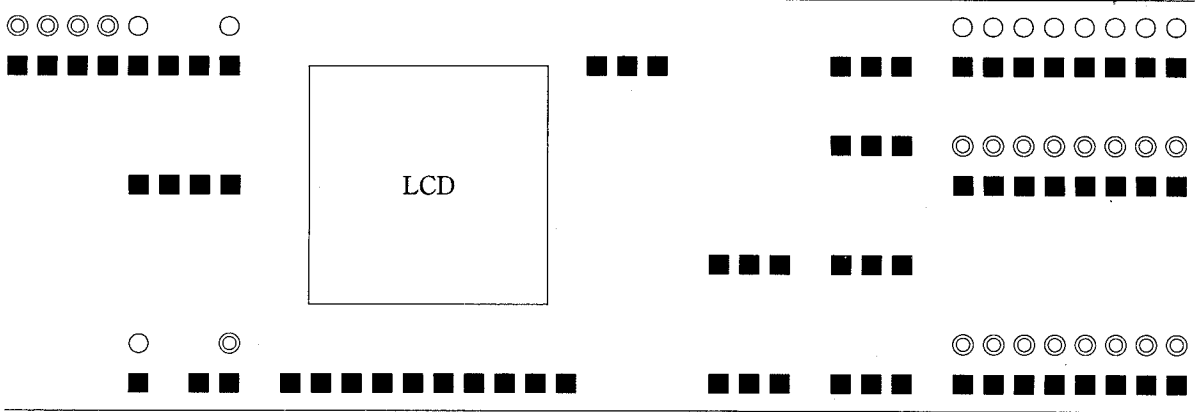
\* 08: LED Check

Check that each red LED blinks once in succession from the left end of the unit (refer to the diagram shown below) and then verify that all red LEDs blink together. Next, check that each green LED blinks once, and then all green LEDs blink together. The currently blinking LEDs will be displayed in the LCD as follows.

\* 08: LED Check      REC   RED   On

(e.g. The red RECORD LED is blinking)

Check that all LEDs blink. (21 of the 32 LEDs are dual-color red/green LEDs)



Note: (◎) indicates a dual-color LED.    (○) indicates a single-color LED.

**TEST END**

Press [EXIT] to end the test. The SY99 will then be waiting for the entry of a test number.

**9. TEST 9: PANEL SWITCH TEST**

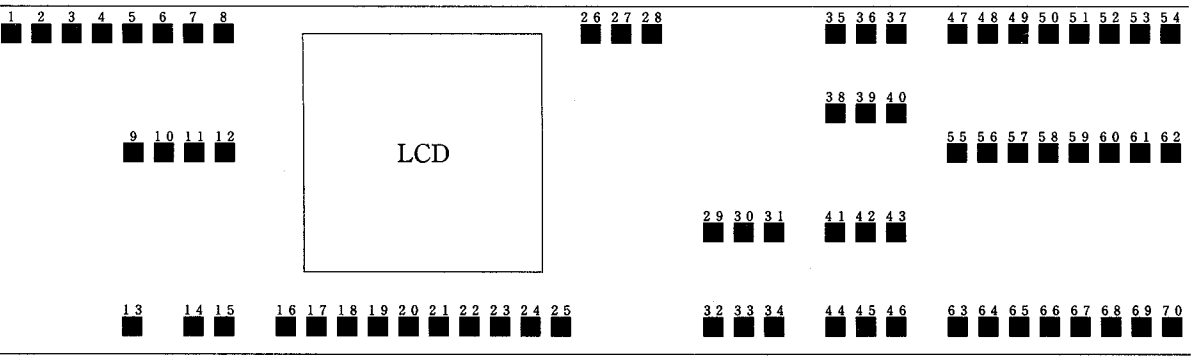
\* 09: Panel Switch

Press the panel switches consecutively from the [VOICE] switch to switch [16], according to the order indicated by the LCD display.

\* 09: Panel Switch      Push REC

(e.g. When checking [RECORD])

The switch pressing order is displayed in the diagram below. If the switch is OK, a beep will sound and you should proceed to test the next switch. If the wrong switch is pressed an unexpected code is sent from the PKS CPU, and the error message NG will be displayed and no sound will be heard. At this time, if the correct switch is pressed then the proper code is received. You will then be able to proceed to test the next switch. The display will indicate OK, if all switches are good.



**DISPLAY OF TEST RESULTS**

OK	<div>* 09: Panel Switch      Push 16      OK</div>
NG	<div>* 09: Panel Switch      Push REC   1? Err</div>

**TEST END**

When switch [16] is pressed, OK is displayed and the test will end. During the test, if NG is detected, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

**10. TEST 10: PITCH BEND WHEEL TEST**

* 10: Pitch Bend	50	99
------------------	----	----

According to the target value displayed on the LCD, slowly move the pitch bend wheel. Check that the value changes from 50 to 99 then to 00 and back to 50 (in other words, center to top then to bottom and back to center).

* 10: Pitch Bend	xx	yy
------------------	----	----

(where xx = current pitch bend value and yy = next target value)

**DISPLAY OF TEST RESULTS**

OK	* 10: Pitch Bend	50	50	OK
----	------------------	----	----	----

NG	* 10: Pitch Bend	xx	Center	NG
----	------------------	----	--------	----

(If the pitch bend value at the beginning or end of the test is not center, then xx indicates the pitch bend value when NG was detected)

**TEST END**

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

**11. TEST 11: MODULATION WHEEL 1 TEST**

* 11: Modulation WH1	00	20-80
----------------------	----	-------

According to the target value displayed on the LCD, slowly move modulation wheel 1. Check that the value changes from 00→20→80→99 then back down to 80→20→00 (in other words, from bottom to top the back to the bottom).

* 11: Modulation WH1	xx	yy
----------------------	----	----

* 11: Modulation WH1	xx	yy-zz
----------------------	----	-------

(where xx = current value of modulation wheel 1, yy and zz are the next target values)

**DISPLAY OF TEST RESULTS**

OK	* 11: Modulation WH1	00	00	OK
----	----------------------	----	----	----

NG (No change in display message)

**TEST END**

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

**12. TEST 12: MODULATION WHEEL 2 TEST**

* 12: Modulation WH2	50	99
----------------------	----	----

Before beginning this test, move modulation wheel 2 to the center position. According to the target value displayed on the LCD, slowly move modulation wheel 2. Check that the value changes from 50 to 99 then to 00 and back to 50 (in other words, from center to top then to bottom and back to center).

* 12: Modulation WH2	xx	yy
----------------------	----	----

* 12: Modulation WH2	xx	yy-zz
----------------------	----	-------

(where xx=current value of modulation wheel 2, yy and zz are the next target values)

**DISPLAY OF TEST RESULTS**

OK	* 12: Modulation WH2	50	50	OK
----	----------------------	----	----	----

NG (No change in display message)

**TEST END**

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

**13. TEST 13: DATA ENTRY SLIDER TEST**

* 13: Data Entry	00	20-80
------------------	----	-------

According to the target value displayed on the LCD, slowly move the data entry slider. Check that the value changes from 00→20→80→99 and the back down to 80→20→00 (in other words, from the bottom to the top and back down to the bottom).

* 13: Data Entry	xx	yy
------------------	----	----

* 13: Data Entry	xx	yy-zz
------------------	----	-------

(where xx=current value of data entry, yy and zz are the next target values)

**DISPLAY OF TEST RESULTS**

OK	* 13: Data Entry	00	00	OK
----	------------------	----	----	----

NG (No change in display message)

**TEST END**

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".



14. TEST 14: ROTARY ENCODER (DATA ENTRY WHEEL) TEST

\* 14: R-Encoder      Right   00

Rotate the rotary encoder (data entry wheel) to the right as indicated by the LCD display. Check that the value on the LCD changes from Right 00→Left 00→Left 01 (in other words, first rotate to the right then to the left).

\* 14: R-Encoder      Right   xx

\* 14: R-Encoder      Left    xx

(where xx = current value)

DISPLAY OF TEST RESULTS

OK      \* 14: R-Encoder      Left   01      OK

NG      (No change in display message)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

15. TEST 15: KEYBOARD TEST

\* 15: Keyboard Check

Play a scale on the keyboard from E0 to G6 with a steady and even touch.

\* 15: Keyboard Check   Push   C1

(e.g. in the case of C1)

If the key switch is ok, the note will sound and you should proceed to play the next key. If you play the wrong key this will produce an unexpected code to the PKS CPU and Err will be displayed. As a result the sound of that note will not be heard. However, if the right key is played following the playing of the wrong key, then correct code is received and the note for that key will sound. You can then proceed to play the next key. If all key switches are good then OK will be displayed on the LCD.

DISPLAY OF TEST RESULTS

OK      \* 15: Keyboard Check   Push   G6      OK

NG      \* 15: Keyboard Check   Push   xxx 17 Err

(if play the wrong key)

NG      \* 15: Keyboard Check   Push   xxx \$nn NG

(if the initial touch was incorrect)

TEST END

When you play the G6 key and OK is displayed, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

**16. TEST 16: AFTERTOUCH TEST**

* 16: After Touch	00	20-80
-------------------	----	-------

According to the target value displayed on the LCD, press a key on the keyboard. Check that the value changes from 00→20→80→99 and back down to 80→20→00 (in other words, apply light pressure and increase pressure to a heavier touch then decrease back to a light touch).

* 16: After Touch	xx	yy
-------------------	----	----

* 16: After Touch	xx	yy-zz
-------------------	----	-------

(where xx = the current aftertouch value, yy and zz are the next target values)

**DISPLAY OF TEST RESULTS**

OK

* 16: After Touch	00	00	OK
-------------------	----	----	----

NG (No change in display message)

**TEST END**

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

**17. TEST 17: MIDI TEST**

* 17: MIDI (I/O/I)
--------------------

After connecting the MIDI IN to the MIDI OUT via a MIDI cable, execute the test. The following message will appear on the LCD.

* 17: MIDI (I/O/I)	Tx:yy	Rx:zz
--------------------	-------	-------

**TEST END**

When you press [EXIT] the test will end and the SY99 will wait for a test number to be entered. If an NG error occurs, because unexpected data was received, the test will end at that point. If an NG error occurs because no data was received within a certain time, the test will continue until [EXIT] is pressed.

**18. TEST 18: DATA CARD INSERT TEST**

* 18: D-Card Insert	0
---------------------	---

Insert a RAM card (MCD64) into the DATA card slot and execute the test. Check that when you remove and insert the card back into the slot, the number on the display changes from 0 to 1 and that the OK result is displayed.

**DISPLAY OF TEST RESULTS**

OK

* 18: D-Card Insert	1	OK
---------------------	---	----

NG (No change in display message)

**TEST END**

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

19. TEST 19: DATA CARDS READ/WRITE TEST

\* 19: D-Card R/Write

This performs a read/write test on the following addresses of the RAM card.  
CARD 1 : 20000h– 27FFFh      CARD 2 : 28000h– 2FFFFh  
Insert a RAM card with the memory protect turned off and execute the test.

DISPLAY OF TEST RESULTS

OK	<div>* 19: D-Card R/Write    CARD : 12      OK</div>
NG	<div>* 19: D-Card R/Write    CARD : x      NG</div>

(e.g. if CARD 2 is No Good)

TEST END

After displaying the results, the test will end. All card data is preserved.

20. TEST 20: DATA CARD PROTECT SWITCH TEST

\* 20: D-Card Protect    0

Use a RAM card to check that the card protect switch status is being read. Check that when the switch is set from “protect off” to “protect on”, the number on the display changes from 0 to 1 and that the OK result is also displayed.

DISPLAY OF TEST RESULTS

OK	<div>* 20: D-Card Protect    1      OK</div>
NG	(No change in display)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, “B. PROCEEDING THROUGH THE TESTS”.

21. TEST 21: RAM BACKUP BATTERY TEST

\* 21: D-Card Battery

This test checks that the voltage of the RAM card backup battery.

DISPLAY OF TEST RESULTS

OK	<div>* 21: D-Card Battery    #.#V      OK</div>
NG	<div>* 21: D-Card Battery    #.#V    Low    NG</div>
	<div>* 21: D-Card Battery    #.#V    High    NG</div>

TEST END

Ends after displaying the test results.

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**22. TEST 22: WAVEFORM CARD INSERT TEST**

* 22: W-Card Insert	0
---------------------	---

Check that when a waveform card is inserted into the slot, the number on the display changes from 0 to 1 and that the OK result is displayed.

**DISPLAY OF TEST RESULTS**

OK

* 22: W-Card Insert	1
---------------------	---

OK

NG

(No change in display)

**TEST END**

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

**23. TEST 23: WAVE ROM READ TEST**

* 23: W-ROM Read
------------------

This test is utilized by the factory and it is not intended for field service use.

**24. TEST 24: WAVE RAM READ/WRITE TEST**

* 24: W-RAM
-------------

This performs a read/write test on the following addresses of the wave RAMs.

Internal WAVE RAM :	400000h – 43FFFFh	Expansion WAVE RAM 1 :	440000h – 47FFFFh
Expansion WAVE RAM 2 :	480000h – 4BFFFFh	Expansion WAVE RAM 3 :	4C0000h – 4FFFFFh
Expansion WAVE RAM 4 :	500000h – 53FFFFh	Expansion WAVE RAM 5 :	540000h – 57FFFFh

And then checks the voltage of the backup battery of the internal WAVE RAM and the expansion WAVE RAMs.

**DISPLAY OF TEST RESULTS**

OK

* 24: W-RAM	000000
-------------	--------

OK

NG

* 24: W-RAM	XORBOX
-------------	--------

NG

The LCD will indicate that the error is occurred by displaying the alphabet R, B, O or X.

R : Only the read/write test is NG.

O : The read/write test and the battery check are OK.

B : Only the battery check is NG.

X : The read/write test and the battery check are NG.

**TEST END**

After displaying the results, the test will end. All RAM data is preserved.

**25. TEST 25: DISK READ/WRITE TEST**

* 25: Disk Read/Write
-----------------------

Use a blank disk to test the disk format. This test will write and read two types of data. Testing is performed on the following tracks.

SIDE 0 : TRACK 40 (sector 4) – TRACK 00 (sector 1) – TRACK 79 (sector 9)  
SIDE 1 : TRACK 40 (sector 4) – TRACK 00 (sector 1) – TRACK 79 (sector 9)

Insert a blank disk with the write protect off and execute the test.

DISPLAY OF TEST RESULTS

OK	* 25: Disk Read/Write C79:H1 Verlfy OK
NG	* 25: Disk Read/Write Cyy:Hx nnnnnnn NG

(where x = side or head number, yy = track or cylinder number, and nnnnnn: condition at time of error)

TEST END

After displaying the results, the test will end.

26. TEST 26: DISK EJECT TEST

* 26: Disk Eject	0
------------------	---

Insert a blank disk and execute the test. Check that when the eject button is pressed and the disk is removed, the number on the display changes from 0 to 1 and that the OK result is displayed.

DISPLAY OF TEST RESULTS

OK	* 26: Disk Eject	1	OK
NG	(No change in display message)		

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

27. TEST 27: BREATH CONTROLLER TEST

* 27: Breath Control	99 00
----------------------	-------

Connect a breath controller and blow into it. Check that the number on the display changes from 00→01→20→80→95→99→80→20→01→00 (in other words, off to strong and back to off).

* 27: Breath Control	xx	yy-zz
----------------------	----	-------

(where xx=current breath control value, yy and zz are the next target values)

DISPLAY OF TEST RESULTS

OK	* 27: Breath Control	xx	00	OK
	(where xx=breath controller value at end of test)			
NG	(No change in display)			

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".



**28. TEST 28: FOOT VOLUME TEST**

* 28: Foot Volume	00	20-80
-------------------	----	-------

Connect a foot controller and operate it throughout its range. Check that the number on the display changes from 00→01→20→80→95→99→95→80→20→01→00 (in other words, starting from the raised position then to the lowered position and back to the raised position).

* 28: Foot Volume	xx	yy-zz
-------------------	----	-------

(where xx = current foot volume value, yy and zz are the next target values)

**DISPLAY OF TEST RESULTS**

OK

* 28: Foot Volume	xx	00	OK
-------------------	----	----	----

(where xx = foot volume value at end of test)

NG

(No change in display)

**TEST END**

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

**29. TEST 29: FOOT CONTROLLER TEST**

* 29: Foot Control	00	20-80
--------------------	----	-------

Connect a foot controller and operate it throughout its range. Check that the number on the display changes from 00→01→20→80→95→99→95→80→20→01→00 (in other words, starting from the raised position then to the lowered position and back to the raised position).

* 29: Foot Control	xx	yy-zz
--------------------	----	-------

(where xx = current foot controller value, yy and zz are the next target values)

**DISPLAY OF TEST RESULTS**

OK

* 29: Foot Control	xx	00	OK
--------------------	----	----	----

(where xx = foot controller value at end of test)

NG

(No change in display)

**TEST END**

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

**30. TEST 30: SUSTAIN SWITCH TEST**

* 30: Sustain	1
---------------	---

Connect a sustain switch and press it on and off. Check that the number on the display changes from 1 to 0 then back to 1 and verify that the OK result is displayed.

**DISPLAY OF TEST RESULTS**

OK

\* 30: Sustain

1

OK

NG

(No change in display)

**TEST END**

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

**31. TEST 31: FOOT SWITCH TEST**

\* 31: Foot Switch

1

Connect a foot switch and press it on and off. Check that the number on the display changes from 1 to 0 then back to 1 and verify that the OK result is displayed.

**DISPLAY OF TEST RESULTS**

OK

\* 31: Foot Switch

1

OK

NG

(No change in display)

**TEST END**

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

**32. TEST 32: 1 kHz FM SOUND OUTPUT (OUTPUT L1) TEST**

\* 32: 1KHz to L1-&gt; L1

Check that the correct signal is output from OUTPUT L1 and PHONES (L) jacks.

The signal route is as follows:

The digital representation of the 1 kHz signal is output from SO0 terminal (channel 0) of OPS3 IC (IC220) to INDV1 terminal (channel 13) of the M3 IC (IC256). From the INDV1 terminal of the M3 IC, the signal is sent to the IN1 terminal of the PAN(2) IC (IC215). From the PAN(2) IC, the signal is output from the S1 and S2 terminals. The signal is then sent to the MXI0 and the MXI1 inputs of the MIX5 IC (IC228). Now the signal is sent out of the MIX5 IC via the MXO0 and the MXO1 terminals which feeds the signal to the SI1 and SI2 inputs of the AFDO (FLOATING POINT CONVERTER) IC (IC206). The AFDO and the DAC work together to produce the analog that is output from the CH1 (Channel 1) terminal. The signal goes to the analog circuits and is output from the OUTPUT L1 jack. It should be noted that the active low FMSEL signal must be at a 0 volt or LOW logic level in order to output this signal.

**ITEMS TO CHECK**

Insert the appropriate 1/4" phone plugs into each output jack and check OUTPUT L1, OUTPUT L2, OUTPUT R1, OUTPUT R2, and PHONES (L/R) outputs. If necessary, verify the frequency, output waveform, output level, and THD of each output using a frequency counter, oscilloscope, AC voltmeter (with 12.47 kHz filter) and distortion meter. The volume control must be set at maximum for these checks. While sounding, the LCD will display the following message:

\* 32: 1KHz to L1-&gt; L1 Output On

Listed below are the specifications and conditions of each output during this test.

OUTPUT L1 : 1kHz  $\pm$  1.5Hz, sine wave, distortion 0.2%, 0.0dB  $\pm$  2dB (10k ohm load)

OUTPUT L2 : less than - 70dB

OUTPUT R1 : less than - 70dB

OUTPUT R2 : less than - 70dB

PHONES (L) : 1kHz, sine wave, distortion 0.2% or less, +5.5dB  $\pm$  2dB (150 ohm load)  
 PHONES (R) : less than -60dB

#### TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 32: 1KHz to L1-> L1 Output Off

### 33. TEST 33: 1kHz FM SOUND OUTPUT (OUTPUT R1) TEST

\* 33: 1KHz to R1-> R1

#### ITEMS TO CHECK

Check that the correct signal is output from OUTPUT R1 and the PHONES (R) jacks.

The basic signal route is the same as it was in TEST 32 except the signal is output from the CH2 (Channel 2) of the AFDO IC.

Insert the appropriate 1/4" phone plugs into each output jack and check OUTPUT L1, OUTPUT L2, OUTPUT R1, OUTPUT R2, and PHONES (L/R) outputs. If necessary, verify the frequency, output waveform, output level, and THD of each output using the previously specified test equipment (refer to TEST 32). The volume control must be set at maximum for these checks. While sounding, the LCD will display the following message:

\* 33: 1KHz to R1-> R1 Output On

Listed below are the specifications and conditions of each output during this test.

OUTPUT R1 : 1kHz  $\pm$  1.5Hz, sine wave, distortion 0.2%, 0.0dB  $\pm$  2dB (10k ohm load)

OUTPUT R2 : less than -70dB

OUTPUT L1 : less than -70dB

OUTPUT L2 : less than -70dB

PHONES (L) : less than -60dB

PHONES (R) : 1kHz, sine wave, distortion 0.2% or less, +5.5dB  $\pm$  2dB (150 ohm load)

#### TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 33: 1KHz to R1-> R1 Output Off

### 34. TEST 34: 1kHz FM SOUND OUTPUT (OUTPUT L2) TEST

\* 34: 1KHz to L2-> L2

#### ITEMS TO CHECK

Check that the correct signal is output from OUTPUT L2 and the PHONES (L) jacks.

The basic signal route is the same as it was in TEST 32 except the signal is output from the CH3 (Channel 3) of the AFDO IC.

Insert the appropriate 1/4" phone plugs into each output jack and check OUTPUT L1, OUTPUT L2, OUTPUT R1, OUTPUT R2, and PHONES (L/R) outputs. If necessary, verify the frequency, output waveform, output level, and THD of each output using the previously specified test equipment (refer to TEST 32). The volume control must be set at maximum for these checks. While sounding, the LCD will display the following message:

\* 34: 1KHz to L2-> L2 Output On

Listed below are the specifications and conditions of the output during this test.

OUTPUT L2 : 1kHz  $\pm$  1.5Hz, sine wave, distortion 0.2%, 0.0dB  $\pm$  2dB (10k ohm load)

OUTPUT L1 : less than -70dB

OUTPUT R1 : less than -70dB

OUTPUT R2 : less than -70dB

PHONES (L) : 1kHz, sine wave, distortion 0.2% or less, +5.5dB  $\pm$  2dB (150 ohm load)

#### TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 34: 1KHz to L2-> L2 Output Off

### 35. TEST 35: 1kHz FM SOUND OUTPUT (OUTPUT R2) TEST

\* 35: 1KHz to R2-> R2

#### ITEMS TO CHECK

Check that the correct signal is output from OUTPUT R2 and the PHONES (R) jacks.

The basic signal route is the same as it was in TEST 32 except the signal is output from the CH4 (Channel 4) of the AFDO IC.

Insert the appropriate 1/4" phone plugs into each output jack and check OUTPUT L1, OUTPUT L2, OUTPUT R1, OUTPUT R2, and PHONES (L/R) outputs. If necessary, verify the frequency, output waveform, output level, and THD of each output using the previously specified test equipment (refer to TEST 32). The volume control must be set at maximum for these checks. While sounding, the LCD will display the following message:

\* 35: 1KHz to R2-> R2 Output On

Listed below are the specifications and conditions of each output during this test.

OUTPUT R2 : 1kHz  $\pm$  1.5Hz, sine wave, distortion 0.2%, 0.0dB  $\pm$  2dB (10k ohm load)

OUTPUT R1 : less than -70dB

OUTPUT L1 : less than -70dB

OUTPUT L2 : less than -70dB

PHONES (R) : 1kHz, sine wave, distortion 0.2% or less, +5.5dB  $\pm$  2dB (150 ohm load)

#### TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 35: 1KHz to R2-> R2 Output Off

### 36. TEST 36: 1kHz FM SOUND OUTPUT (OUTPUT L2 OUTPUT L1) TEST

\* 36: 1KHz to L2-> L1

#### ITEMS TO CHECK

Check that when the plug connected to OUTPUT L2 is pulled out, the signal being output from OUTPUT L2 is now output from OUTPUT L1. The basic signal route is the same as it was for TEST 34.

Insert the appropriate 1/4" phone plug into OUTPUT L1 and verify, if necessary, the frequency, output waveform, output level, and THD of this output using the previously specified test equipment (refer to TEST 32). The volume control must be set at maximum for this test. While sounding, the LCD will display the following message:



\* 36: 1KHz to L2-> L1 Output On

The specifications for this test are as follows:

OUTPUT L1 : 1kHz, sine wave, 0.0dB  $\pm$  2dB (10k ohm load)

#### TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 36: 1KHz to L2-> L1 Output Off

### 37. TEST 37: 1kHz FM SOUND OUTPUT (OUTPUT R2 OUTPUT R1) TEST

\* 37: 1KHz to R2-> R1

#### ITEMS TO CHECK

Check that when the plug connected to OUTPUT R2 is pulled out, the signal being output from OUTPUT R2 is now output from OUTPUT R1. The basic signal route is the same as it was for TEST 35.

Insert the appropriate 1/4" phone plug into OUTPUT R1 and verify, if necessary, the frequency, output waveform, output level, and THD of this output using the previously specified test equipment (refer to TEST 32). The volume control must be set at maximum for this test. While sounding, the LCD will display the following message:

\* 37: 1KHz to R2-> R1 Output Off

The specifications for this test are as follows:

OUTPUT R1 : 1kHz, sine wave, 0.0dB  $\pm$  2dB (10k ohm load)

#### TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 37: 1KHz to R2-> R1 Output Off

### 38. TEST 38: 1kHz FM SOUND OUTPUT (OUTPUT R1→OUTPUT L1) TEST

\* 38: 1KHz to R1-> L1

#### ITEMS TO CHECK

Check that when the plug connected to OUTPUT R1 is pulled out, the signal being output from OUTPUT R1 is now output from OUTPUT L1. The basic signal route is the same as it was for TEST 33.

Insert the appropriate 1/4" phone plug into OUTPUT L1 and verify, if necessary, the frequency, output waveform, output level, and THD of this output using the previously specified test equipment (refer to TEST 32). The volume control must be set at maximum for this test. While sounding, the LCD will display the following message:

\* 38: 1KHz to R1-> L1 Output On

The specifications for this test are as follows:

OUTPUT L1 : 1kHz, sine wave, 0.0dB  $\pm$  2dB (10k ohm load)

**TEST END**

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 38: 1KHz to R1-> L1 Output Off

**39. TEST 39: 1kHz PCM SOUND OUTPUT (EFFECT → OUTPUT L, R) TEST**

\* 39: PCM to Eff Para

**SIGNAL PATH**

The digital representation of 1 kHz signal is output from SO0 terminal (channel 1) of the OPS3 IC (IC218) to DIINO terminal of the M3 IC (IC257). From DIOUT1 and DIOUT2 terminals of the M3 IC, the signal is sent to the SI1 terminal of the ESI ICs (IC222 and IC223). The signal output from the SO1 terminal of ESI IC is sent to the SI0 terminal of the DSP2 ICs (IC226 and IC227).

From the DSP2 ICs, the signal is out from SO0 terminal to the ESI IC and the other DSP2 IC. These signals then sent to the MIX inputs of the MIX5 IC (IC228). Now the signal is sent out of the MIX5 IC via the MXO terminals which feeds the signal to the SI1 and SI2 inputs of the AFD0 IC. The AFD0 and the DAC work together to produce the analog that is output from each output terminals via the analog circuits. It should be noted that the active low FMSEL signal must be at a +5V or HIGH logic level in order to output this signal.

Each effective signal route is as follows:

- OUTPUT L1 : MOD(IC221), DRAM(IC229-IC232), SO0 terminal of DSP2 (IC226), MXO0 terminal (channel L) of MIX5 (IC228)
- OUTPUT R1 : MOD(IC221), DRAM(IC232-IC235), SO1 terminal of DSP2 (IC226), MXO0 terminal (channel R) of MIX5 (IC228)
- OUTPUT L2 : MOD(IC223), DRAM(IC236-IC239), SO0 terminal of DSP2 (IC227), MXO1 terminal (channel L) of MIX5 (IC228)
- OUTPUT R2 : MOD(IC223), DRAM(IC232-IC235), SO1 terminal of DSP2 (IC227), MXO1 terminal (channel R) of MIX5 (IC228)

**ITEMS TO CHECK**

Insert the appropriate 1/4" phone plug into each output jack and verify, if necessary, the frequency, output waveform, output level, and THD of this output using the previously specified test equipment (refer to TEST 32).

The volume control must be set at maximum for this test. While sounding, the LCD will display the following message:

\* 39: PCM to Eff Para      Output On

The specifications for this test are as follows:

- OUTPUT L1 : 1kHz, sine wave, distortion 0.3% or less,  $0.0 \pm 2\text{dBm}$  (10k ohm load)
- OUTPUT R1 : 1kHz, sine wave, distortion 0.3% or less,  $0.0 \pm 2\text{dBm}$  (10k ohm load)
- OUTPUT L2 : 1kHz, sine wave, distortion 0.3% or less,  $0.0 \pm 2\text{dBm}$  (10k ohm load)
- OUTPUT R2 : 1kHz, sine wave, distortion 0.3% or less,  $0.0 \pm 2\text{dBm}$  (10k ohm load)

**TEST END**

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 39: PCM to Eff Para      Output Off

**40. TEST 40: 1kHz FM SOUND OUTPUT (EFFECT → OUTPUT L) TEST**

\* 40: FM to Eff Para

Check that the correct signal is output from OUTPUT L1 and OUTPUT L2 jacks.

The signal route is the same as it was in TEST 39 except for the following:

The signal is output from the SO0 terminal (channel 0) of the OPS3 IC (IC220) to the M3 IC (IC256).

And the FMSEL signal must be at LOW logic level.

**ITEMS TO CHECK**

Insert the appropriate 1/4" phone plug into each output jack and verify, if necessary, the frequency, output waveform and output level using the previously specified test equipment (refer to TEST 32).

The volume control must be set at maximum for this test. While sounding, the LCD will display the following message:

\* 40: FM to Eff Para      Output On

The specifications for this test are as follows:

OUTPUT L1 : 1kHz, sine wave,  $0.0 \pm 2\text{dBm}$  (10k ohm load)

OUTPUT L2 : 1kHz, sine wave,  $0.0 \pm 2\text{dBm}$  (10k ohm load)

**TEST END**

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 40: FM to Eff Para      Output Off

**41. TEST 41: 1kHz FM SOUND OUTPUT (EFFECT → OUTPUT L1) TEST**

\* 41: FM to Eff Seri

Check that the correct signal is output from OUTPUT L1 jacks.

The digital representation of 1 kHz signal is output from SO0 terminal (channel 0) of the OPS3 IC (IC220) to DIINO terminal of the M3 IC (IC256). From DIOU1 and DIOU2 terminals of the M3 IC, the signal is sent. Then the signal output from the SO2 terminal of the DPS2 IC (IC226) is sent to the DSP2 IC (IC227).

From the DSP2 IC (IC227), the signal is sent to the input terminal of the MIX5 IC (IC228). Now the signal is sent out of the MIX5 IC via the MX00 terminal. It should be noted that the FMSEL signal must be at a 0V or LOW logic level, and the MOD ICs, DRAM ICs are not used during this test.

**ITEMS TO CHECK**

Insert the appropriate 1/4" phone plug into OUTPUT L1 jack and verify, if necessary, the frequency, output waveform and output level using the previously specified test equipment (refer to TEST 32).

The volume control must be set at maximum for this test. While sounding, the LCD will display the following message:

\* 41: FM to Eff Seri      Output On

The specifications for this test is as follows:

OUTPUT L1 : 1kHz, sine wave,  $0.0 \pm 2\text{dBm}$  (10k ohm load)

**TEST END**

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 41: FM to Eff Seri      Output Off



**42. TEST 42: AWM (M3) SOUND OUTPUT TEST**

\* 42: PCM Check

**SIGNAL PATH**

This outputs the sound which is stored in addresses 012000h – 01FFFFh of WAVE ROM. The data stored at these addresses is retrieved by the M3(A) IC (IC257) and output via pin 1 (INDV0 terminal, channel 0). The signal from pin 1 is then output to pin 11 (IN0 terminal) of the PAN(1) IC (IC216). The PAN (1) IC outputs the signal from pins 21 and 22 (S1 and S2 terminals, respectively) and sends the signal to pins 12 and 13 (SI2 and S11 terminals, respectively) of the PAN (2) IC (IC215). The PAN (2) IC outputs the signal from pins 21 and 22 (S1 and S2 terminals, respectively) to pins 8 and 7 (MXI0 and MXI1 terminals) of MIX5 (IC228) IC. The signal is sent out of the MIX5 IC via the MXO0 and the MXO1 terminals. This ultimately produces signal output from OUTPUT L1.

**ITEMS TO CHECK**

Confirm that a AWM signal is being sent to OUTPUT L1 using an amplifier and speaker to monitor the signal. The AWM signal is not a steady tone. While this signal is sounding, the LCD will display the following message:

\* 42: PCM Check      Output On

**TEST END**

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 42: PCM Check      Output Off

**43. TEST 43: FM SOUND OUTPUT THROUGH M3 IC (AWM) TEST**

\* 43: FM Thru M3(PCM)

**SIGNAL PATH**

A sine wave which is frequency swept by the EGM2 (1) IC will cause signals to be alternately output from OUTPUT L1, OUTPUT R1, OUTPUT L2 and OUTPUT R2 in a two channel pair sequence. The FMSEL signal to the EGM2 (1) and OPS3 (1) must be at a 1 or HIGH logic level for this test. The appropriate data from EGM2 (1) IC (IC217) is sent to the OPS3 (1) IC (IC218) in order to produce the sound. The OPS3 (1) IC outputs the signals from pins 54 and 55 (SO0, channel 1 and SO1, channel 9) via IC225 (pins 8 and 9) to pins 27 and 28 (terminals DIIN0 and DIIN1) of the M3 (A) IC (IC257). The M3 (A) IC outputs the signals from pins 1 and 2 (INDV0, channel 5 and INDV1, channel 6) to pins 10 and 11 (IN1 and IN0 terminals) of the PAN (1) IC (IC216). The PAN (1) IC sends the signals out from pins 21 and 22 (S1 and S2 terminals) to pins 12 and 13 (ST2 and ST1 terminals) of the PAN (2) IC (IC215). The PAN (2) IC outputs the signals from pins 21 and 22 (S1 and S2 terminals) to pins 8 and 7 (MXI0 and the MXI1 terminals) of MIX5 IC (IC228). The signal is sent out of the MIX5 IC via the MXO0 and the MXO1 terminals. This ultimately produces signal output from OUTPUT L1, OUTPUT R1, OUTPUT L2, OUTPUT R2.

**ITEMS TO CHECK**

Insert the appropriate 1/4" phone plug into OUTPUT L1 and observe the output waveform with an oscilloscope. Check that the level does not change excessively as the output sweeps through its frequency range. The volume control must be set at comfortable listening level for this test. While sounding, the LCD will display the following message.

\* 43: FM Thru M3(PCM)      Output On

**TEST END**

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 43: FM Thru M3(PCM) Output Off

**44. TEST 44: FM SOUND OUTPUT THROUGH M3 IC (DIGITAL FILTER) TEST**

\* 44: FM Thru M3(FM)

**SIGNAL PATH**

A sine wave which is frequency swept by the EGM2 (2) IC will cause signals to be alternately output from OUTPUT L1, OUTPUT R1, OUTPUT L2 and OUTPUT R2 in a two channel pair sequence. The FMSEL signal to the EGM2 (2) must be at a 0 or LOW logic level and the OPS3 (2) must be at a 1 or HIGH logic level for this test. The appropriate data from EGM2 (2) IC (IC219) is sent to the OPS3 (2) IC (IC220) in order to produce the sound. The OPS3 (2) IC outputs the signals from pins 54 and 55 (SO0, channel 0 and SO1, channel 8) via IC225 (pins 8 and 9) to pins 27 and 28 (terminals DIINO and DIIN1) of the M3 (B) IC (IC256). The M3 (B) IC outputs the signals from pins 1 and 2 (INDV0, channel 14 and INDV1, channel 15) to pins 10 and 11 (IN1 and IN0 terminals) of the PAN (2) IC (IC215). The PAN (2) IC sends the signals out from pins 21 and 22 (S1 and S2 terminals) to pins 8 and 7 (MXI0 and MXI1 terminals) of MIX5 IC. The signal is sent out of the MIX5 IC via the MXO0 and the MXO1 terminals. This ultimately produces signal output from OUTPUT L1, OUTPUT R1, OUTPUT L2, OUTPUT R2.

**ITEMS TO CHECK**

Insert the appropriate 1/4" phone plug into OUTPUT L1 and observe the output waveform with an oscilloscope. Check that the level does not change excessively as the output sweeps through its frequency range. The volume control must be set at a comfortable listening level for this test. While sounding, the LCD will display the following message.

\* 44: FM Thru M3(FM) Output On

**TEST END**

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 44: FM Thru M3(FM) Output Off

**45. TEST 45: FM SOUND OUTPUT FEEDBACK THROUGH M3 IC TEST**

\* 45: Feedback FM->M3

The basic signal path is the same as it was for TEST 43 except for the following:

The frequency swept sine wave produced by the EGM2 (1) and OPS3 (1) will be fed back from the M3 (A) IC to the OPS3 (1) IC. As in TEST 43, the output signals will occur alternately in a two channel pair sequence. For this test, the signals from pins 1 and 2 (INDV0 and INDV1 terminals) of M3 (A) IC (IC257) will be fed back to pins 69 and 70 (SI0 and SI1 terminals) of OPS3 (1) IC (IC218).

**ITEMS TO CHECK**

Insert the appropriate 1/4" phone plug into OUTPUT L1 and observe the output waveform with an oscilloscope. Check that the level does not change excessively as the output sweeps through its frequency range. It should be noted that due to the feedback condition of this test there may be a slight amount of distortion present in the output signal. The volume control must be set at a comfortable listening level for this test. While sounding, the LCD will display the following message:

\* 45: Feedback FM->M3 Output On

### TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 45: Feedback FM Output Off

## 46. TEST 46: HIGH CLICK SOUND TEST

\* 46: Click High

### ITEMS TO CHECK

Check that a high click signal is properly output from OUTPUT L1, OUTPUT L2, OUTPUT R1 and OUTPUT R2. Make sure that the click volume control is set to maximum. While sounding, the LCD will display the following message:

\* 46: Click High Click On

Verify that the high click signal is sent to each output by using an amplifier and speaker to monitor signal. Insert the appropriate 1/4" phone plugs into OUTPUT L1, OUTPUT L2, OUTPUT R1 and OUTPUT R2 and observe the output waveform with an oscilloscope. Check that the output waveform is a rounded square wave with an approximate peak-to-peak voltage of 500mV.

### TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 46: Click High Click Off

## 47. TEST 47: LOW CLICK SOUND TEST

\* 47: Click Low

### ITEMS TO CHECK

Check that a low click signal is properly output from OUTPUT L1. Make sure that the click volume control is set to maximum. While sounding, the LCD will display the following message:

\* 47: Click Low Click On

Verify that the low click signal is sent to OUTPUT L1 by using an amplifier and speaker to monitor signal. Insert the appropriate 1/4" phone plugs into OUTPUT L1, OUTPUT L2, OUTPUT R1 and OUTPUT R2 and observe the output waveform with an oscilloscope. Check that the output waveform is a rounded square wave with an approximate peak-to-peak voltage of 500mV.

### TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY99 will wait for the entry of a test number.

\* 47: Click Low Click Off



**48. TEST 48: JACKS ALL OFF TEST**

* 48: Jack All Off
--------------------

Connect the Sustain and Foot Switch pedals to the appropriate jacks. With nothing connected to the Foot Volume, Foot Controller, and Breath controller jacks, check that the following display appears.

* 48: Jack All Off	SU FS
--------------------	-------

Then while pressing the foot switches connected to the Sustain and Foot Switch jacks, remove the pedal plugs, and check that the display shows "OK".

**DISPLAY OF TEST RESULTS**

OK	* 48: Jack All Off	OK
NG	* 48: Jack All Off	FV NG

(e.g. if the foot volume jack is NG)

**TEST END**

The result is displayed and the test will end.

**49. TEST 49: FACTORY SET TEST**

* 49: Factory Set
-------------------

This test is used to initialize the data listed below to the factory settings:

Synthesizer system data  
64-internal voice data  
16-internal multi data  
Sequencer setup data

When this test is executed, the following display will appear.

* 49: Factory Set	[NO] or [YES] ?
-------------------	-----------------

If you press [YES], the factory preset data will be restored.

If you press [NO], they will not be restored.

**DISPLAY OF TEST RESULTS**

If factory settings are restored.

OK	* 49: Factory Set	OK
----	-------------------	----

If not restored there will be no change in the display as shown below.

* 49: Factory Set	[NO] or [YES] ?
-------------------	-----------------

**TEST END**

The LCD displays the results, the factory preset data will be restored, and the test will then end. After the factory preset data has been restored, the system data will be as follows:

\*\*\*\*\*

## SYNTH

\*\*\*\*\*

Note Shift.....+0  
 Fine Turning .....+0  
 Fixed Velocity.....off  
 Velocity Curve .....0(normal)  
 Assignable Foot Switch .....65  
 Assignable Wheel .....13  
 Edit Confirm .....on  
 Kbd Trans Ch .....1

Voice Recv Ch.....1  
 Local on/off.....on  
 Note on/off .....all  
 Device Number .....all  
 Bulk Protect .....on  
 Program Change.....on  
 Pattern Protect .....on  
 MDR Memory .....0Kbyte

## ----- Greeting Message -----

"Create YOUR sound !"  
 "...I'm ready"

## ----- PAN factory set -----

I1~I32 = P1 ~P32

## ----- MCT factory set -----

I 1 = P62(Far East)  
 I 2 = P63(Blue)

## ----- VOICE -----

I-A01~D16 =P1-A01~D16

## ----- MULTI -----

I-01~16 =P1-01~16

\*\*\*\*\*

## SEQUENCER

\*\*\*\*\*

record quantize .....0(off)  
 click sw .....1(rec)  
 click beat .....0(1/4)  
 record type .....over  
 sync .....0(internal)  
 receive .....KBD  
 filter velocity .....1(on)  
 filter control change .....1(on)  
 filter pitch bend .....1(on)  
 filter program change .....1(on)  
 filter after touch.....0(off)  
 filter exclusive .....1(on)

midi control .....1(on)  
 click/beat .....1/96  
 accent1 value .....24  
 accent2 value .....56  
 accent3 value .....88  
 accent4 value .....120  
 gate type .....1(normal)

**50. TEST 50: EXIT TEST PROGRAM**

\* 50: Exit

When this is executed, the following display will appear.

\* 50: Exit                      [NO] or [YES] ?

To exit the test program mode, press the [YES] switch. To remain in the test program mode press the [NO] switch. This will cause the SY99 to wait for the entry of a test number.

**DISPLAY OF TEST RESULTS**

If test mode is not exited.

\* 50: Exit                      [NO] or [YES] ?



## ■テストプログラム

### A. テストエントリー

本体の電源立ち上げ後、数秒待ち、次の操作をする。

[VOICE]を押しながら[BANK D]を押しさらに[8]を押すと、次の画面が表示される。

```
*** SY99 TEST Ver #.## *** Please Select

Main ROM : Version #.## 1990-10-??
SEQ. ROM : Version #.## 1990-10-??

[-1] : AUTO          [+1] : MANUAL

[ COPY ] : Fact.set   [EXIT] : Exit
```

[-1]、[+1]、[COPY]および[EXIT]を使用してテストモードの選択を行う。

[+1]を押すと、マニュアルモードで、テストにエントリーされる。

[COPY]を押すと、“49. ファクトリーセット”を実行した後、自動的にテストモードから抜け、プレイモードになる。

[EXIT]を押すとテストモードを抜け、プレイモードになる。

### B. テストの進め方

テストにエントリーすると、まず、次の画面が表示される。

```
*** SY99 TEST Ver #.## *** MODE : MANUAL

* 01 : ROM CHECK
  02 : RAM Read/Write
  03 : SEQUENCER ROM
  04 : SEQUENCER RAM
  05 : RAM Battery
```

[+1]、[-1]、[ENTER]、[COPY]、[PAGE+]、[PAGE-]、[EXIT]、[TEN KEY]およびロータリーエンコーダーを使用してテストを進める。

[+1]を押すと、現在選択されているテストの次のテストが実行される。

[-1]を押すと、現在選択されているテストの一つ前のテストが実行される。

[ENTER]を押すと、現在選択されているテストが実行される。

[PAGE+]を押すと、現在選択されているテストの次のテストが選択され、テスト項目が表示される。

[PAGE-]を押すと、現在選択されているテストの一つ前のテストが選択され、テスト項目が表示される。

[EXIT]を押すと、“50. EXIT”が実行される。

[TEN KEY 0]から[TEN KEY 9]を使用して、2桁の数字を入力することにより、テストの選択が行える。

#### バージョン表示モード；

[Voice]→[INT]→[1]を押す。MAIN ROMとSEQ ROMのバージョンが表示され、[EXIT]によって、本体プログラムへ復帰する。

#### NGと判断した時のテストの進めかた

次の各テストにおいて、NGと判断した場合、以下に示す操作により、テストナンバー待ち状態にでき、もう一度テストを行うか、他のテストを行う事が出来る。

9. パネルスイッチ
10. ピッチベンド
11. モジュレーションホイール1
12. モジュレーションホイール2

13. データエントリー
14. ロータリーエンコーダー
15. キーボード
16. アフタータッチ
17. MIDI IN/OUT
18. カードインサート
20. カードプロテクトスイッチ
22. ウェーブカードインサート
26. ディスクイジェクト
27. プレスコントロール
28. フットボリューム
29. フットコントロール
30. サステーン
31. フットスイッチ
48. ジャック オール オフ

[EXIT]を押すと、テストナンバー待ち状態となる。

ただし、"9. パネルスイッチ"の[EXIT]のテストの場合には、この方法は、対応していない。

## 0. INITIAL TEST

テストに使用するH8内蔵RAM h'FB80-h'FF7F  
DM2シート M3×2 よりのIRQ (DM2 BUS TEST)。  
テストプログラムエントリー時、自動的に実施。

### 判定結果の表示

OK 特に無し

NG \*WORK RAM ERROR

\*\* IC128(RAM) ERROR,TEST CONTINUE? \*\*

\*M3 IRQ

\* M3 IRQ CHECK ERROR,TEST CONTINUE? \*

### テストの終了方法

[YES]を押す

## 1. SYSTEM ROM

\* 01; ROM CHECK

ROMのリードテストを行う。次の6つのアドレスに対してテストを行う。

IC111 =h'80000-h'8000F

IC111 =h'A0000-h'A000F

IC111 =h'C0000-h'C000F

IC111 =h'E0000-h'E000F

IC112 =h'60000-h'6000F

IC113 =h'10000-h'1000F

(ROMテストは16byteのみCheck)

### 判定結果の表示

OK

\* 01: ROM CHECK

OK

NG

\* 01: ROM CHECK

n:ICxxx

NG

(ROM n がNGの場合、xxx : NGとなったICの番号)

### テストの終了方法

判定を表示、出力して終了する。

## 2. SYSTEM RAM

\* 02: RAM Read/Write

RAMのリード/ライトテストを行う。次のICのアドレスに対してテストを行う。

IC119 =h'40000-h'5FFFF

IC115 =h'30000-h'37FFF

### 判定結果の表示

OK

\* 02: RAM Read/Write

OK

NG

\* 02: RAM Read/Write IC119

NG

### テストの終了方法

判定を表示、出力して終了する。

すべての RAMのデータは保存される。

## 3. SEQUENCER ROM

\* 03: SEQUENCER ROM

ROMのリードテストを行う。次のICのアドレスに対してテストを行う。

IC101=h'8000-h'BFFFで#0-#6の7BANK

IC101=h'C000-h'FFFFで#7の1BANK

### 判定結果の表示

OK

\* 03: SEQUENCER ROM

OK

NG

\* 03: SEQUENCER ROM

NG

### テストの終了方法

判定を表示、出力して終了する。

## 4. SEQUECER RAM

\* 04: SEQUENCER RAM

RAMのリード/ライトテストを行う。次のICの全アドレスに対してテストを行う。

1: IC103=h'4000-h'5FFF

2: IC102=h'6000(WINDOW 0),h'6200(WINDOW 1),h'6400(WINDOW 2),h'6600(WINDOW 3)

### 判定結果の表示

OK

\* 04: SEQUENCER RAM

OK

NG

\* 04: SEQUENCER RAM ICxxx

NG

(ICxxx:NGとなったICの番号)

### テストの終了方法

判定を表示、出力して終了する。

すべての RAMのデータは保存される。

## 5. Battery

\* 05: RAM Battery

RAMバックアップバッテリー電圧が、2.9V以上3.3V以下を確認する。

### 判定結果の表示

OK      \* 05: RAM Battery      3.2V      OK

NG      \* 05: RAM Battery      #.#V      Low      NG

\* 05: RAM Battery      #.#V      High      NG

### テストの終了方法

判定を表示、出力して終了する。

## 6. LCDドット黒

\* 06: LCD All On

全ドットが黒に変化していることを確認する。コントラストVRで、コントラスト調整が出来る事。

### テストの終了方法

[EXIT]を押すと、テストは終了し、次の画面を表示して、テストナンバー待ち状態になる。

\* 06: LCD All On

## 7. LCDドット白

\* 07: LCD All Off

全ドットが白に変化していることを確認する。

### テストの終了方法

[EXIT]を押すと、テストは終了し、次の画面を表示して、テストナンバー待ち状態になる。

\* 07: LCD All Off

## 8. LED順次点燈・全点燈

\* 08: LED Check

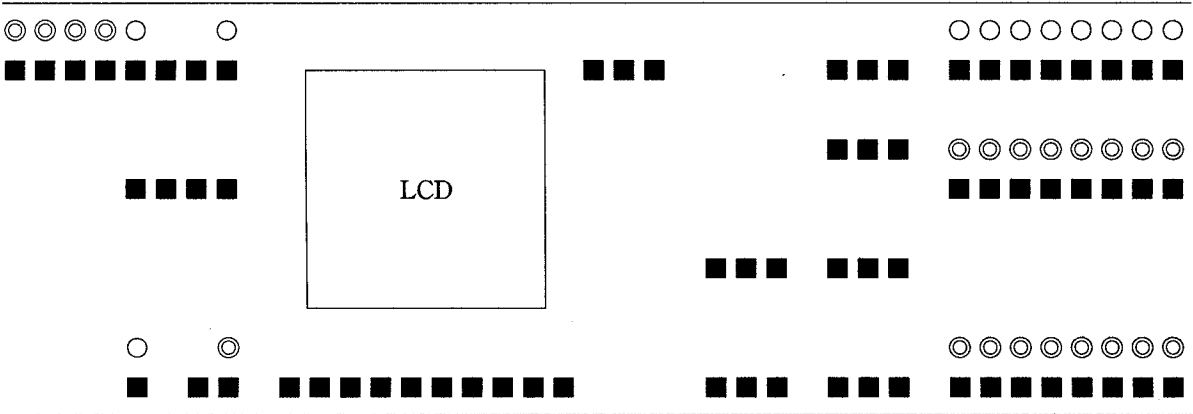
次の図の左から順に赤LEDが1回点滅した後、すべての赤色のLEDが同時に点燈し、次に緑LEDが1回点滅した後、すべての緑色のLEDが同時に点燈することを確認する。現在点滅しているLEDが以下の様にLCDに表示される。

\* 08: LED Check      REC    RED    On

(RECORDの赤色のLEDが点滅している場合)

すべてのLEDが点滅することを確認する。(32個中21個は赤/緑の2色)





注) ◎印は、2色のLEDを示す。○印は、単色のLEDを示す。

テストの終了方法  
[EXIT]を押すと、その時点の各LEDの点燈/消燈の状態のままテストは終了し、テストナンバー待ち状態になる。

9. パネルスイッチ

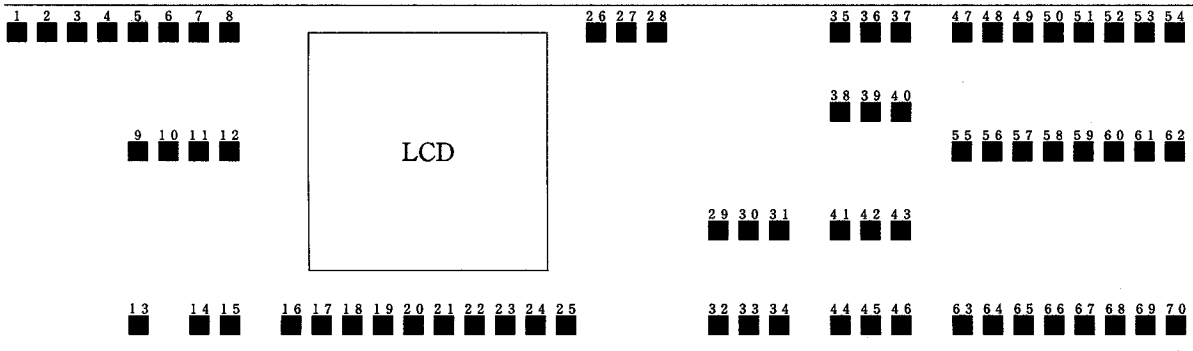
\* 09: Panel Switch

[VOICE]から[16]までのパネルスイッチを、以下の様なLCDの表示に従ってON/OFFする。

\* 09: Panel Switch      Push REC

([Record]のチェックの場合)

チェックの順序を下図に示す。  
正常な場合、"ポーッ"と発音して、次のスイッチのテストに進む。  
期待されないコードがPKSより送られると、NGが表示され発音しない。  
その後、正しいコードが受信されると、次のスイッチのテストに進む。  
すべてのスイッチが正常であれば、OKが表示される。



判定結果の表示

OK      \* 09: Panel Switch      Push 16      OK

NG      \* 09: Panel Switch      Push REC      1? Err

テストの終了方法  
[16]までチェックすると、OKが表示され、テストは終了する。  
テスト途中で、NGと判断した場合の処理方法は、"B. テストの進めかた"を参照のこと。

## 10. ピッチベンド

* 10: Pitch Bend	50	99
------------------	----	----

ピッチベンドを、以下の様なLCD表示に従って50-99-00-50(中央-上-下-中央)と滑らかに動かす。

* 10: Pitch Bend	xx	yy
------------------	----	----

xx;現在のピッチベンドの値

yy;次の目標値

引っ掛りがなく、数字が滑らかに変化し、OKの判定が出ることを確認する。

## 判定結果の表示

OK	* 10: Pitch Bend	50	50	OK
----	------------------	----	----	----

NG	* 10: Pitch Bend	xx	Center	NG
----	------------------	----	--------	----

テスト開始時および終了時にピッチベンドの値がCenterでなかった場合、xx:NG判定時のピッチベンドの値

## テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、“B. テストの進めかた”を参照のこと。

## 11. モジュレーションホイール1

* 11: Modulation WH1	00	20-80
----------------------	----	-------

モジュレーションホイール1を、以下の様なLCD表示に従って00-20-80-99-20-80-00(下-上-下)と滑らかに動かす。

* 11: Modulation WH1	xx	yy
----------------------	----	----

* 11: Modulation WH1	xx	yy-zz
----------------------	----	-------

xx :現在のモジュレーションホイール1の値

yy, yy-zz :次の目標値

引っ掛りがなく、数字が滑らかに変化し、OKの判定が出ることを確認する。

## 判定結果の表示

OK	* 11: Modulation WH1	00	00	OK
----	----------------------	----	----	----

NG 表示なし

## テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、“B. テストの進めかた”を参照のこと。

## 12. モジュレーションホイール2

* 12: Modulation WH2	50	99
----------------------	----	----

検査を始める前にモジュレーションホイール2の位置を中央にセットしておく。

モジュレーションホイール2を、以下の様なLCD表示に従って50-99-00-50(中央-上-下-中央)と滑らかに動かす。

* 12: Modulation WH2	xx	yy
----------------------	----	----

* 12: Modulation WH2	xx	yy-zz
----------------------	----	-------

xx ; 現在のモジュレーションホイール2の値

yy, yy-zz ; 次の目標値

引っ掛りがなく、数字が滑らかに変化し、OKの判定が出ることを確認する。

## 判定結果の表示

OK

* 12: Modulation WH2	50	50	OK
----------------------	----	----	----

NG

表示なし

## テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、“B. テストの進めかた”を参照のこと。

## 13. データエントリー

* 13: Data Entry	00	20-80
------------------	----	-------

データエントリーを、以下の様なLCD表示に従って00-20-80-99-20-80-00(下-上-下)と滑らかに動かす。

* 13: Data Entry	xx	yy
------------------	----	----

* 13: Data Entry	xx	yy-zz
------------------	----	-------

xx ; 現在のデータエントリーの値

yy, yy-zz ; 次の目標値

引っ掛りがなく、数字が滑らかに変化し、OKの判定が出ることを確認する。

## 判定結果の表示

OK

* 13: Data Entry	00	00	OK
------------------	----	----	----

NG

表示なし

## テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、“B. テストの進めかた”を参照のこと。

## 14. ロータリーエンコーダー

* 14: R-Encoder	Right	00
-----------------	-------	----

ロータリーエンコーダーを、以下の様なLCD表示に従って00-01-00-01(右回転、左回転)と動かす。

* 14: R-Encoder	Right	xx
-----------------	-------	----

* 14: R-Encoder	Left	xx
-----------------	------	----

xx; 現在の値

引っ掛りがなく、OKの判定が出ることを確認する。

#### 判定結果の表示

OK	* 14: R-Encoder	Left	01	OK
----	-----------------	------	----	----

NG	表示なし			
----	------	--	--	--

#### テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、“B. テストの進めかた”を参照のこと。

### 15. キーボード

* 15: Keyboard Check
----------------------

E0からG6まで76鍵を、以下の様なLCDの表示に従い、イニシャルタッチh'10-h'6Fの強さでスケーリングする。

* 15: Keyboard Check	Push	C1
----------------------	------	----

(C1のチェックの場合)

正常な場合、キーON音を出力し、次のキーのチェックへ進む。

期待されないコードがPKSより送られると、NGが表示されSINE波は出力されないが、その後、正しいコードが受信されると、キーON音を出力し、次のキーのチェックへ進む。

すべてのキーが正常であれば、OKが表示される。

#### 判定結果の表示

OK	* 15: Keyboard Check	Push	G6	OK
----	----------------------	------	----	----

NG	* 15: Keyboard Check	Push	xxx !? Err
----	----------------------	------	------------

(期待されないコードがPKSより送られて来た場合)

* 15: Keyboard Check	Push	xxx \$nn NG
----------------------	------	-------------

(イニシャルタッチが正常でない場合)

#### テストの終了方法

G6までチェックすると、OKが表示され、テストは終了する。

テスト途中で、NGと判断した場合の処理方法は、“B. テストの進めかた”を参照のこと。

### 16. アフタータッチ

* 16: After Touch	00	20-80
-------------------	----	-------

アフタータッチを、以下の様なLCD表示に従って

00-20-80-99-20-80-00(弱-強-弱)と鍵盤を押す。

* 16: After Touch	xx	yy
-------------------	----	----



* 16: After Touch	xx	yy-zz
-------------------	----	-------

xx ; 現在のアフタータッチの値

yy, yy-zz ; 次の目標値

引っ掛かりがなく、数字が滑らかに変化し、OKの判定が出ることを確認する。

#### 判定結果の表示

OK	* 16: After Touch	00	00	OK
----	-------------------	----	----	----

NG	表示なし
----	------

#### テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、"B. テストの進めかた"を参照のこと。

### 17. MIDI IN/OUT

* 17: MIDI (I/O/T)
--------------------

IN、OUTをMIDIケーブルで接続した後、テストを実行する。

LCDには、以下の様に表示が行われる。

* 17: MIDI (I/O/T)	Ix:yy	Rx:zz
--------------------	-------	-------

#### テストの終了方法

[EXIT]を押すと、テストは終了し、テストナンバー待ち状態になる。

期待されないデータが受信されたため、NGとなった場合、その時点でテストは終了する。

一定時間内に受信が終了しないため、NGとなった場合は、[EXIT]が押されるまでテストは続けられる。

### 18. カードインサート

* 18: D-Card Insert	0
---------------------	---

テスト用カードをスロットに挿入し、テストを実行する。カードを抜いて再度入れた時、数字が0から1に変化し、OKの判定が出ることを確認する。

#### 判定結果の表示

OK	* 18: D-Card Insert	1	OK
----	---------------------	---	----

NG	表示なし
----	------

#### テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、"B. テストの進めかた"を参照のこと。

### 19. カードリードライト

* 19: D-Card R/Write
----------------------

テスト用カードを使用して、次の2つのアドレスに対してカードのリード/ライト テストを行う。

CARD 1 = h'20000 - h'27FFF

CARD 2 = h'28000 - h'2FFFF

メモリープロテクトをオフにしたテスト用カードを差し込み、テストを実行させる。

## 判定結果の表示

OK	* 19: D-Card R/Write CARD : 12	OK
----	--------------------------------	----

NG	* 19: D-Card R/Write CARD : x	NG
----	-------------------------------	----

(CARD 2が NG の場合)

## テストの終了方法

判定を表示、出力して終了する。

すべてのCARD上のデータは保存される。

## 20. カードプロテクトスイッチ

* 20: D-Card Protect 0
------------------------

テスト用カードを使用して、カードプロテクトスイッチの状態を読み込めることを確認する。スイッチを操作して、プロテクトオフからプロテクトオン状態にした時、数字が0から1に変化しOKの判定が出ることを確認する。

## 判定結果の表示

OK	* 20: D-Card Protect 1	OK
----	------------------------	----

NG	表示なし
----	------

## テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、「B. テストの進めかた」を参照のこと。

## 21. カードバッテリー

* 21: D-Card Battery
----------------------

RAMカードバックアップバッテリー電圧が、測定できることを確認する。

## 判定結果の表示

OK	* 21: D-Card Battery #.#V	OK
----	---------------------------	----

NG	* 21: D-Card Battery #.#V Low	NG
----	-------------------------------	----

* 21: D-Card Battery #.#V High	NG
--------------------------------	----

## テストの終了方法

判定を表示、出力して終了する。

## 22. ウェーブカードインサート

* 22: W-Card Insert 0
-----------------------

テスト用ウェーブカードをスロットに入れた時、数字が0から1に変化し、OKの判定が出ることを確認する。

## 判定結果の表示

OK	* 22: W-Card Insert 1	OK
----	-----------------------	----

NG 表示なし

## テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、“B. テストの進めかた”を参照のこと。

## 23. ウェーブROMリード

* 23: W-ROM Read
------------------

本テストは、工業出荷検査用のため、ここでは実行しません。

## 24. ウェーブ RAM

* 24: W-RAM
-------------

インターナショナルWAVE RAM、拡張WAVE RAM のリード/ライトテストを行う。

テストするアドレスは、

インターナショナルWAVE RAM :h'400000-h'43FFFF

拡張WAVE RAM1 :h'440000-h'47FFFF

拡張 WAVE RAM2 :h'480000-h'4BFFFF

拡張WAVE RAM3 :h'4C0000-h'4FFFFF

拡張 WAVE RAM4 :h'500000-h'53FFFF

拡張WAVE RAM5 :h'540000-h'57FFFF

インターナショナルWAVE RAM、拡張WAVE RAMのバッテリーチェックを行う。

## 判定結果の表示

OK	* 24: W-RAM 000000	OK
----	--------------------	----

NG	* 24: W-RAM XORBOX	NG
----	--------------------	----

テスト結果は、インターナショナルWAVE RAM、拡張WAVE RAM 1～5 の順に記号で表示する。記号は、

R : リード/ライト テストのみNG      B : バッテリーチェックのみNG

O : 両方ともOK      X : 両方ともNG

## テストの終了方法

判定を表示、出力して終了する。

すべてのRAMのデータは保存される。

## 25. ディスクリードライト

* 25: Disk Read/Write
-----------------------

生ディスクを使用して、ディスクのフォーマット/リード/ライトを2種類のDataに対してテストを行う。

次のトラックに対してテストを行う。

SIDE 0 = 40(SEC 4) - 00(SEC 1) - 79(SEC 9)

SIDE 1 = 40(SEC 4) - 00(SEC 1) - 79(SEC 9)

メモリープロテクトをオフにした生ディスクを差し込み、テストを実行させる。

## 判定結果の表示

OK	* 25: Disk Read/Write C79:H1 Verify OK
----	--

NG	* 25: Disk Read/Write Cyy:Hx nnnnnnn NG
----	---

(x ; side番号、yy ; トラック番号)

(nnnnnn ; エラー時の状態)

## テストの終了方式

判定を表示、出力して終了する。

## 26. ディスクイジェクト

* 26: Disk Eject	0
------------------	---

生ディスクを挿入してテストを実行する。

イジェクトボタンを押しディスクを取り出した時、数字が0から1に変化し、OKの判定が出ることを確認する。

## 判定結果の表示

OK	* 26: Disk Eject	1	OK
----	------------------	---	----

NG 表示なし

## テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、“B. テストの進めかた”を参照のこと。

## 27. ブレスコントロール

* 27: Breath Control	99 00
----------------------	-------

ブレスコントローラーを接続し、以下の様なLCD表示に従って00-01-20-80-95-99-20-80-00-01(止-強-止)のシュミレーションをする。

* 27: Breath Control	xx	yy-zz
----------------------	----	-------

xx ; 現在のブレスコントロールの値

yy,yy-zz ; 次の目標値

数字が滑らかに変化し、OKの判定が出ることを確認する。

## 判定結果の表示

OK	* 27: Breath Control	xx	00	OK
----	----------------------	----	----	----

xx ; テスト終了時のブレスコントロールの値

NG 表示なし

## テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、“B. テストの進めかた”を参照のこと。



## 28. フットボリューム

* 28: Foot Volume	00	20-80
-------------------	----	-------

フットボリュームを接続し、以下の様なLCD表示に従って00-01-20-80-95-99-20-80-00-01(上げる-踏み込む-上げる)と滑らかに動かす。

* 28: Foot Volume	xx	yy-zz
-------------------	----	-------

xx ; 現在のフットボリュームの値

yy, yy-zz ; 次の目標値

数字が滑らかに変化し、OKの判定が出ることを確認する。

## 判定結果の表示

OK	* 28: Foot Volume	xx	00	OK
----	-------------------	----	----	----

xx ; テスト終了時のフットボリュームの値

NG 表示なし

## テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、“B. テストの進めかた”を参照のこと。

## 29. フットコントロール

* 29: Foot Control	00	20-80
--------------------	----	-------

フットコントロールを接続し、以下の様なLCD表示に従って00-01-20-80-95-99-20-80-00-01(上げる-踏み込む-上げる)と滑らかに動かす。

* 29: Foot Control	xx	yy-zz
--------------------	----	-------

xx ; 現在のフットコントロールの値

yy, yy-zz ; 次の目標値

数字が滑らかに変化し、OKの判定が出ることを確認する。

## 判定結果の表示

OK	* 29: Foot Control	xx	00	OK
----	--------------------	----	----	----

xx ; テスト終了時のフットコントロールの値

NG 表示なし

## テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、“B. テストの進めかた”を参照のこと。

## 30. サステイーン

* 30: Sustain	1
---------------	---

サステイーンペダルを接続し、ON/OFFする。この時、数字が1-0-1と変化し、OKの判定が出ることを確認する。

## 判定結果の表示

OK	* 30: Sustain	1	OK
----	---------------	---	----

NG 表示なし

## テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、“B. テストの進めかた”を参照のこと。

## 31. フットスイッチ

* 31: Foot Switch	1
-------------------	---

フットペダルを接続し、ON/OFFする。この時、数字が1-0-1と変化し、OKの判定が出ることを確認する。

## 判定結果の表示

OK	* 31: Foot Switch	1	OK
----	-------------------	---	----

NG 表示なし

## テストの終了方法

判定を表示、出力して終了する。

テスト途中で、NGと判断した場合の処理方法は、“B. テストの進めかた”を参照のこと。

## 32. 1kHz OUTPUT L1発音(FM)

* 32: 1KHz to L1-> L1
-----------------------

OUTPUT L1およびPHONES(L)より正常な信号が出力されていることを確認する。

なお信号源は、FMSEL=L-OPS3(IC220)のS00(CH0)-M3(IC256)のINDV1(CH13)-PAN(IC215)のS1, S2-MIX5(IC228)のMXO1,2のルートを使っている。

OUTPUT L1、OUTPUT L2、OUTPUT R1、OUTPUT R2、PHONES(L)、PHONES(R) 共にジャックを差し込み、各出力の周波数、出力波形、出力レベルを周波数カウンタ、オシロスコープ、レベル計(12.47kHzフィルター付き)、歪率計で観測する。

マスターボリュームはmaxとする。発音中は、LCD表示が以下の様になる。

* 32: 1KHz to L1-> L1 Output On
---------------------------------

## チェック項目

OUTPUT L1 ; 1kHz $\pm$ 1.5Hz、sine波、歪率 0.2%、0.0 $\pm$ 2dbm(負荷10kohm)

OUTPUT L2 ; -70dbm以下

OUTPUT R1 ; -70dbm以下

OUTPUT R2 ; -70dbm以下

PHONES(L) ; 1kHz、sine波、歪率 0.2%、+5.5 $\pm$ 2dbm(負荷150ohm)

PHONES(R) ; -60dbm以下

## テストの終了方法

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

* 32: 1KHz to L1-> L1 Output Off
----------------------------------

## 33. 1kHz OUTPUT R1 発音(FM)

\* 33: 1KHz to R1-> R1

OUTPUT R1および PHONES(R) より正常な信号が出力されていることを確認する。

なお信号源は、TEST 32と同じ。

OUTPUT L1、OUTPUT L2、OUTPUT R1、OUTPUT R2、PHONES(L)、PHONES(R)共にジャックを差し込み、各出力の出力波形、出力レベルを、オシロスコープ、レベル計(12.47kHzフィルター付き)、歪率計で観測する。

マスターボリュームはmaxとする。発音中は、LCD表示が以下の様になる。

\* 33: 1KHz to R1-> R1 Output On

## チェック項目

OUTPUT R1 ; 1kHz、sine波、歪率 0.2%、 $0.0 \pm 2\text{dbm}$ (負荷10kohm)

OUTPUT L1 ; -70dbm以下

OUTPUT R2 ; -70dbm以下

OUTPUT L2 ; -70dbm以下

PHONES(R) ; 1kHz、sine波、歪率0.2%、 $+5.5 \pm 2\text{dbm}$ (負荷150ohm)

PHONES(L) ; -60dbm以下

## テストの終了方法

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 33: 1KHz to R1-> R1 Output Off

## 34. 1kHz OUTPUT L2 発音(FM)

\* 34: 1KHz to L2-> L2

OUTPUT L2およびPHONES(L) より正常な信号が出力されていることを確認する。

なお信号源は、TEST 32と同じ。

OUTPUT L1、OUTPUT L2、OUTPUT R1、OUTPUT R2、PHONES(L)、PHONES(R)共にジャックを差し込み、各出力の出力波形、出力レベルをオシロスコープ、レベル計(12.47kHzフィルター付き)、歪率計で観測する。

マスターボリュームはmaxとする。発音中は、LCD表示が以下の様になる。

\* 34: 1KHz to L2-> L2 Output On

## チェック項目

OUTPUT L2 ; 1kHz、sine波、歪率 0.2%、 $0.0 \pm 2\text{dbm}$ (負荷10kohm)

OUTPUT L1 ; -70dbm以下

OUTPUT R1 ; -70dbm以下

OUTPUT R2 ; -70dbm以下

PHONES(L) ; 1kHz、sine波、歪率0.2%、 $+5.5 \pm 2\text{dbm}$ (負荷150ohm)

## テストの終了方法

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 34: 1KHz to L2-> L2 Output Off

## 35. 1kHz OUTPUT R2 発音(FM)

\* 35: 1KHz to R2-> R2

OUTPUT R2および PHONES(R) より正常な信号が出力されていることを確認する。

なお信号源は、TEST 32と同じ。

OUTPUT L1、OUTPUT L2、OUTPUT R1、OUTPUT R2、PHONES(L)、PHONES(R)共にジャックを差し込み、各出力の出力波形、出力レベルをオシロスコープ、レベル計(12.47kHzフィルター付き)、歪率計で観測する。

マスターボリュームはmaxとする。発音中は、LCD表示が以下の様になる。

\* 35: 1KHz to R2-> R2 Output On

## チェック項目

OUTPUT R2 ; 1kHz波、sine波、歪率0.2%、 $0.0 \pm 2\text{dbm}$ (負荷10kohm)

OUTPUT L1 ;  $-70\text{dbm}$ 以下

OUTPUT L2 ;  $-70\text{dbm}$ 以下

OUTPUT R1 ;  $-70\text{dbm}$ 以下

PHONES(R) ; 1kHz、sine波、歪率0.2%、 $+5.5 \pm 2\text{dbm}$ (負荷150ohm)

## テストの終了方法

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 35: 1KHz to R2-> R2 Output Off

## 36. L MONO

\* 36: 1KHz to L2-> L1

OUTPUT L2より出力されている信号がOUTPUT L2のプラグを抜いた時、OUTPUT L1より出力されることを確認する。なお信号源は、TEST 32と同じ。

OUTPUT L1にジャックを差し込み、出力波形、出力レベルを、オシロスコープ、レベル計(12.47kHzフィルター付き)で観測する。

マスターボリュームはmaxとする。発音中は、LCD表示が以下の様になる。

\* 36: 1KHz to L2-> L1 Output On

## チェック項目

OUTPUT L1 ; 1kHz、sine波、 $0.0 \pm 2\text{dbm}$ (負荷10kohm)

## テストの終了方法

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 36: 1KHz to L2-> L1 Output Off

## 37. R MONO

\* 37: 1KHz to R2-> R1

OUTPUT R2より出力されている信号がOUTPUT R2のプラグを抜いた時、OUTPUT R1より出力されることを確認する。なお信号源は、TEST 32と同じ。

OUTPUT R1にジャックを差し込み、出力波形、出力レベルを、オシロスコープ、レベル計(12.47kHzフィルター付き)で観測する。

マスターボリュームはmaxとする。発音中は、LCD表示が以下の様になる。

\* 37: 1KHz to R2-> R1 Output Off



## チェック項目

OUTPUT R1 ; 1kHz, sine波,  $0.0 \pm 2\text{dbm}$  (負荷10kohm)

## テストの終了方法

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 37: 1KHz to R2-> R1 Output Off

## 38. L R MONO

\* 38: 1KHz to R1-> L1

OUTPUT R1より出力されている信号がOUTPUT R1のプラグを抜いた時、OUTPUT L1より出力されることを確認する。なお信号源は、TEST 32と同じ。

OUTPUT L1にジャックを差し込み、出力波形、出力レベルを、オシロスコープ、レベル計 (12.47kHzフィルター付き) で観測する。

マスターボリュームはmaxとする。発音中は、LCD表示が以下の様になる。

\* 38: 1KHz to R1-> L1 Output On

## チェック項目

OUTPUT L1 ; 1kHz, sine波,  $0.0 \pm 2\text{dbm}$  (負荷10kohm)

## テストの終了方法

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 38: 1KHz to R1-> L1 Output Off

## 39. PCM to Effect Parallel

\* 39: PCM to Eff Para

Effectを通ったPCM側の信号が、OUTPUT L1,OUTPUT R1,OUTPUT L2,OUTPUT R2より正常に出力されていることを確認する。

なお信号源は、FMSEL=H-OPS3(IC218)のSO0(CH1)-M3(IC257)のDIOU1,2-DSP2(IC226,IC227)のSO0,1-MIX5(IC228)のMXO0,1のルートを使用。

DSP2は、それぞれのMOD,DRAMを通して出力されます。

2基のDSP2の接続はパラレルです。Effect部の信号経路は下記のとおり。

OUTPUT L1=MOD(IC221),DRAM(IC229-232),DSP2(IC226)のSO0-MIX5のMXO0-L

OUTPUT R1=MOD(IC221),DRAM(IC232-235),DSP2(IC226)のSO1-MIX5のMXO0-R

OUTPUT L2=MOD(IC223),DRAM(IC236-239),DSP2(IC227)のSO0-MIX5のMXO0-L

OUTPUT R2=MOD(IC223),DRAM(IC239-242),DSP2(IC227)のSO1-MIX5のMXO0-R

OUTPUT L1、OUTPUT R1、OUTPUT L2、OUTPUT R2 にジャックを差し込み (他はオープン)、出力波形、出力レベルを、オシロスコープ、レベル計 (12.47kHz フィルター付き)、歪率計で観測する。

マスターボリュームはmaxとする。発音中は、LCD表示が以下の様になる。

\* 39: PCM to Eff Para Output On

## チェック項目

OUTPUT L1 ; 1kHz, sine波, 歪率0.3%,  $0.0 \pm 2\text{dbm}$  (負荷10kohm)

OUTPUT R1 ; 1kHz, sine波, 歪率0.3%,  $0.0 \pm 2\text{dbm}$  (負荷10kohm)

OUTPUT L2 ; 1kHz, sine波, 歪率0.3%,  $0.0 \pm 2\text{dbm}$  (負荷10kohm)

OUTPUT R2 ; 1kHz, sine波, 歪率0.3%,  $0.0 \pm 2\text{dbm}$  (負荷10kohm)

**テストの終了方法**

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 39: PCM to Eff Para      Output Off

**40. FM to Effect Parallel**

\* 40: FM to Eff Para

Effectを通ったFM側の信号が、OUTPUT L1、OUTPUT L2より正常に出力されていることを確認する。

信号源は、FMSEL=L-OPS3(IC220)のSO0(CH0)-M3(IC256)のDIOU0,1-DSP2(IC226,227)のSO0,1のルートを使っています。

Effect部はTEST39と同じです。

OUTPUT L1、OUTPUT R1、OUTPUT L2、OUTPUT R2 にジャックを差し込み(他はオープン)、出力波形、出力レベルを、オシロスコープ、レベル計(12.47kHz フィルター付き)で観測する。

マスターボリュームは max とする。発音中は、LCD 表示が以下の様になる。

\* 40: FM to Eff Para      Output On

**チェック項目**

OUTPUT L1 ; 1kHz、sine波、 $0.0 \pm 2\text{dbm}$ (負荷10kohm)

OUTPUT L2 ; 1kHz、sine波、 $0.0 \pm 2\text{dbm}$ (負荷10kohm)

**テストの終了方法**

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 40: FM to Eff Para      Output Off

**41. FM to Effect Seri**

\* 41: FM to Eff Seri

シリアル接続されたエフェクトを通った信号がOUTPUT L1に正常に出力されている事を確認する。

尚信号源は、FMSEL=L-OPS3(IC220)のSO0(CHO) - M3(IC256)のDIOU0,1-DSP2(IC226)のSO2 - DSP2(IC227)のSO0 - MIX5(IC228)のMXO0のルートを使用。MOD、DRAMは使用していない。2基のDSP2の接続はシリアルです。

OUTPUT L1にジャックを差し込み(他はオープン)、出力波形、出力レベルをオシロスコープ、レベル計(12.47kHz フィルター付き)で観測する。

マスターボリュームはmaxとする。発音中は、LCD表示が以下のようなになる。

\* 41: FM to Eff Seri      Output On

**チェック項目**

OUTPUT L1 ; 1kHz、sine波、 $0.0 \pm 2\text{dbm}$  (負荷10kohm)

**テストの終了方法**

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 41: FM to Eff Seri      Output Off

## 42. PCM Check

\* 42: PCM Check

WAVE ROM 012000番地～01FFFF番地に記録されている音を、M3(IC257), INDV0端子(CH0)-PAN(IC216) S1, S2-PAN(IC215) S1, S2-MIX5(IC228)のMXO0,1を通してOUTPUT L1に出力する。  
OUTPUT L1 にジャックを差し込み、OUTPUT L1の出力波形を観測する。  
マスターボリュームはmaxとする。発音中は、LCD表示が以下の様になる。

\* 42: PCM Check      Output On

## チェック項目

聴感

## テストの終了方法

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 42: PCM Check      Output Off

## 43. FM Thru M3(PCM)

\* 43: FM Thru M3(PCM)

EGM2で周波数 SWEEPされた正弦波をL1, R1, L2, R2各端子より2ch分交互に出力する。音源は、FMSEL=H-EGM2(IC217)-FMSEL=H-OPS3(IC218)のSO0(CH1), SO1(CH9)-M3(IC257)のINDV0(CH5),INDV1(CH6)-PAN(IC216)のS1, S2-PAN(IC215)のS1, S2-MIX5(IC228)のMXO0,1のルートを使用している。  
OUTPUT L1にジャックを差し込み、出力波形を観測する。又、レベルが周波数SWEEPに対し著しく変化しない事を確認する。  
マスターボリュームはmaxとする。発音中は、LCD表示が以下の様になる。

\* 43: FM Thru M3(PCM)      Output On

## チェック項目

聴感

## テストの終了方法

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 43: FM Thru M3(PCM)      Output Off

## 44. FM Thru M3(FM)

\* 44: FM Thru M3(FM)

EGM2で周波数 SWEEPされた正弦波をL1, R1, L2, R2各端子より2ch分交互に出力する。音源は、FMSEL=L-EGM2(IC219)-FMSEL=H-OPS3(IC220)のSO0(CH0), SO1(CH8)-M3(IC256)のINDV0(CH14),INDV1(CH15)-PAN(IC215)のS1, S2-MIX5(IC228)のMXO0,1のルートを使用している。  
OUTPUT L1にジャックを差し込み、出力波形を観測する。又、レベルが周波数SWEEPに対し著しく変化しない事を確認する。  
マスターボリュームはmaxとする。発音中は、LCD表示が以下の様になる。

\* 44: FM Thru M3(FM)      Output On

## チェック項目

聴感

**テストの終了方法**

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 44: FM Thru M3(FM) Output Off

**45. Feedback FM- M3**

\* 45: Feedback FM->M3

EGM2で周波数 SWEEPされた正弦波が、M3を通してフィードバックされる。2ch分交互に出力される。音源は、TEST 43と同じ、但しM3(IC257)のINDV0, INDV1の信号がOPS3(IC218)のSI0,SI1端子にフィードバックされる。

OUTPUT L1にジャックを差し込み、出力波形を観測する。

特にフィードバックされて歪みっぽい音である事を確認する。

マスターボリュームはmaxとする。発音中は、LCD表示が以下の様になる。

\* 45: Feedback FM->M3 Output On

**チェック項目**

聴感

**テストの終了方法**

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 45: Feedback FM Output Off

**46. ハイクリック発音**

\* 46: Click High

OUTPUT L1, L2, R1, R2 より正常なハイクリック信号が出力されていることを確認する。

OUTPUT L1、OUTPUT R1、OUTPUT L2、OUTPUT R2共にジャックを差し込み、OUTPUT L1, R1, L2, R2 の出力波形をオシロスコープで観測する。

クリックボリュームはmaxとする。発音中は、LCD表示が以下の様になる。

\* 46: Click High Click On

**チェック項目**

聴感により、ハイクリックと判別がつくことを確認する。

出力波形が、なまった方形波であることを確認する。

500mVp-p

**テストの終了方法**

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 46: Click High Click Off

**47. ロークリック発音**

\* 47: Click Low

OUTPUT L1より正常なロークリック信号が出力されていることを確認する。

OUTPUT L1、OUTPUT R1、OUTPUT L2、OUTPUT R2 共にジャックを差し込み、OUTPUT L1 の出力波形をオシロスコープで観測する。

クリックボリュームはmaxとする。発音中は、LCD表示が以下の様になる。



\* 47: Click Low      Click On

#### チェック項目

聴感により、ロークリックと判別がつくことを確認する。

出力波形が、なまった方形波であることを確認する。

500mVp-p

#### テストの終了方法

[EXIT]を押すと、次の画面を表示し、発音は終了し、テストナンバー待ち状態になる。

\* 47: Click Low      Click Off

### 48. ジャック オールオフ

\* 48: Jack All Off

サステーン、フットスイッチはプラグを差したままで、フットボリューム、フットコントロール、プレスコントロールのジャックにプラグを差さない状態で、次の状態が表示される事。

\* 48: Jack All Off      SU FS

その後、サステーン、フットスイッチのペダルを踏みながらプラグを抜いた時、"OK"が表示される事を確認する。

#### 判定結果の表示

OK

\* 48: Jack All Off

OK

NG

\* 48: Jack All Off      FV

NG

(フットボリュームのジャックがNGの場合)

#### テストの終了方法

判定を表示し、出力して終了する。

### 49. ファクトリーセット

\* 49: Factory Set

次のデータを、イニシャルデータにセットする。

シンセサイザーシステム

インターナル64ボイス

インターナル16マルチ

シーケンサーセットアップ

テストを実行すると、次の画面が表示される。

\* 49: Factory Set      [NO] or [YES] ?

[YES]を押すと、ファクトリーセットされる。

[NO]を押すと、セットされない。

#### 判定結果の表示

セットされた場合

\* 49: Factory Set

OK

セットされなかった場合

\* 49: Factory Set [NO] or [YES] ?

### テストの終了方法

判定を表示、出力して終了する。

ファクトリーセット終了後、次に示すシステムデータがセットされる。

\*\*\*\*\*

#### SYNTH

\*\*\*\*\*

Note Shift.....+0  
 Fine Turning .....+0  
 Fixed Velocity.....off  
 Velocity Curve .....0(normal)  
 Assignable Foot Switch .....65  
 Assignable Wheel .....13  
 Edit Confirm .....on  
 Kbd Trans Ch .....1  
 Voice Recv Ch.....1  
 Local on/off.....on  
 Note on/off .....all  
 Device Number .....all  
 Bulk Protect .....on  
 Program Change.....on  
 Pattern Protect .....on  
 MDR Memory.....0Kbyte

#### ----- Greeting Message -----

"Create YOUR sound !"  
 " ...I'm ready"

#### ----- PAN factory set -----

I1~I32 = P1 ~P32

#### ----- MCT factory set -----

I 1 = P62(Far East)  
 I 2 = P63(Blue)

#### ----- VOICE -----

I-A01~D16 =P1-A01~D16

#### ----- MULTI -----

I-01~16 =P1-01~16

\*\*\*\*\*

## SEQUENCER

\*\*\*\*\*

record quantize .....0(off)  
 click sw .....1(rec)  
 click beat .....0(1/4)  
  
 record type .....over  
 sync .....0(internal)  
 receive .....KBD  
  
 filter velocity .....1(on)  
 filter control change .....1(on)  
 filter pitch bend .....1(on)  
 filter program change .....1(on)  
 filter after touch .....0(off)  
 filter exclusive .....1(on)  
  
 midi control .....1(on)  
 click/beat .....1/96  
  
 accent1 value .....24  
 accent2 value .....56  
 accent3 value .....88  
 accent4 value .....120  
 gate type .....1(normal)

## 50. EXIT

\* 50: Exit

テストを実行すると、次の画面が表示される。

\* 50: Exit

[NO] or [YES] ?

[YES]を押すと、テストモードから抜ける。

[NO]を押すと、テストナンバー待ち状態になる。

## 判定結果の表示

テストモードから抜けなかった場合

\* 50: Exit

[NO] or [YES] ?

## ■ ERROR MESSAGES

### MIDI

#### **MIDI buffer full !**

When the SY99 attempted to receive or transmit a large amount of MIDI data, its handling capacity was exceeded.

#### **MIDI data error !**

An error occurred when receiving MIDI data.

#### **MIDI checksum error !**

An error occurred when receiving bulk data.

#### **Data empty !**

Sequence data (bulk) was received, but the message contained no data.

#### **Bulk rejected; sample exists !**

An unoccupied sample number could not be found, so the bulk sample data was not received.

#### **Song memory full !**

When receiving sequence data (bulk), the internal memory capacity was exceeded, and not all the data was received.

#### **Device number is off !**

Since the device number is off, bulk data cannot be transmitted or received.

#### **Device number mismatch !**

Since the device numbers did not match, the bulk data was not received.

#### **Bulk canceled !**

While receiving or transmitting bulk data, EXIT was pressed to abort the operation.

### Data card

#### **Data card not ready !**

The data card is not correctly inserted into the slot.

#### **Card protected !**

Since the memory protect switch of the card is on, data cannot be saved to the card.

#### **Illegal format !**

The card is the wrong format.

#### **Verify error !**

The data was not correctly saved.

#### **Illegal size !**

The data card is not of the 64 Kbyte variety accepted by the SY99.

### Wave card

#### **Wave card not ready !**

The wave card is not correctly inserted into the slot.

#### **Different wave card (ID= ) !**

The wave card which is inserted is not the one used by the voice or multi.

#### **ID Number mismatch !**

A multi includes voices which use two or more wave cards.



## Disk

### **Disk not ready !**

The disk is not correctly inserted into the disk drive.

### **Illegal change !**

During the backup operation, the original and back up disks were inserted in the wrong order.

### **Illegal disk !**

The data in the disk is faulty.

### **Bad disk !**

The disk is faulty.

### **File not found !**

The file was not found.

### **Write protected !**

The disk is write protected.

### **Disk full !**

There is no more memory available on the disk.

### **Directory full !**

The directory area on the disk is full, and new files cannot be created.

### **Media type error !**

The disk is the wrong type.

### **Illegal file !**

The file is not for the SY99.

### **Song memory full !**

The sequencer memory is full.

### **Sample memory full !**

The sample memory area is full.

### **MDR memory full !**

The MDR memory area is full.

## Sequencer and display

### **Please stop sequencer !**

The sequencer cannot play during disk or card loading or saving, during bulk data transmission, or during master control setting.

### **Illegal time !**

You attempted to execute the Get Pattern operation, but the time signature was incorrect.

### **Illegal input !**

You attempted to enter an invalid data value in Edit Insert mode.

### **Range is exceeded !**

The parameter you specified in an edit job is beyond the valid range.

### **Data not found !**

When you executed the Search Part operation in Chain Pattern, the specified data was not found.

### **Internal buffer full !**

More sequence data was played back than could be sounded.

## Battery

### **Change internal battery !**

The internal backup battery needs to be replaced.

### **Change card battery !**

The card backup battery needs to be replaced.

### **Change wave BAT !**

The backup battery for the internal MDR/sample RAM area or an expansion memory board (as specified in the message) needs to be replaced.

## Other

### **Use bank D !**

The voice must be stored in bank D.

### **Only C1–C6 data valid !**

You are attempting to save a drum voice to bank A, B, or C. Only the data for notes C1 through C6 will be saved as a result of this operation. Save the voice to bank D if you wish to save the data for all notes E0 through G6.

### **Illegal mark !**

You attempted to mark a display page while using the compare function.

### **Use bank A–C !**

The voice must be stored in bank A, B, or C.

## Sample

### **Please allocate sample memory !**

You attempted to enter Sample utility mode, but no memory has been allocated for sample use. Please use the System utility memory allocate function to allocate memory for sample use.

### **Not enough memory for sample !**

You attempted to reduce the memory area allocated for sample use beyond the minimum required by currently existing samples. Please initialize the sample memory or delete samples before attempting to reduce the amount of MDR/sample RAM allocated for sample use.

### **Over internal waveform number !**

You attempted to load a number of waveforms exceeding the internal memory maximum of 64.

### **Sample data not exists !**

You attempted copy or save sample data from a sample number which does not contain any data.

### **Sample data protected !**

Copy-protected sample data may not be saved to disk or transmitted via MIDI dump.

### **Over sample number !**

You attempted to load a number of samples exceeding the internal memory maximum of 99.

## MDR

### **Please allocate MDR memory !**

You attempted to enter Sample utility mode, but no memory has been allocated for MDR use. Please use the System utility memory allocate function to allocate memory for MDR use.

### **Not enough memory for MDR !**

You attempted to reduce the memory area allocated for MDR use beyond the minimum required by currently existing MDR data. Please initialize the MDR memory or delete MDR data before attempting to reduce the amount of MDR/sample RAM allocated for MDR use.

### **MDR data already exists !**

You attempted to input data to an MDR number already occupied by data. Please choose a different MDR number as the destination for incoming data.

### **MDR data not found !**

You attempted to output data from an empty MDR number.

## ■ エラーメッセージ

MIDI関係	
ディスプレイ表示	メッセージの内容
MIDI buffer full !	一度に多量のMIDIデータが送受信されたため、送受信ができません。データ量を減らしてください。
MIDI data error !	MIDIデータを受信した際、異常がありました。
MIDI checksum err !	バルクデータの受信の際、異常がありました。
Bulk canceled !	シーケンスバルクデータ受信中や、サンプルダンプスタンダード送信中に[EXIT]が押されたので、データの送受信を中止しました。
Bulk protected !	バルクプロテクトがオンになっているため、バルクデータの受信ができません。
Device number is off !	デバイスナンバーがオフになっているため、バルクデータの送受信ができません。
Device number mismatch !	デバイスナンバーのチャンネルが一致していないため、バルクデータの受信ができません。

データカード関係	
ディスプレイ表示	メッセージの内容
Data Card not ready !	カードが本体に正しくセットされていません。
Card protected !	カード自体のプロテクトスイッチがオンになっているため、カードへのデータの書き込みができません。
Illegal format !	カードのフォーマットが違います。
Verify error !	カードのセーブが正しく行われていません。
Illegal size !	カードの容量が64KByte ではありません。
Verity error !	カードの不良で、書き込みができません。

ウェイブカード関係	
ディスプレイ表示	メッセージの内容
Wave card not ready !	ウェイブカードが本体に正しくセットされていません。
Different wave card (ID= ) !	プレイしようとしているボイスで使用するべきウェイブフォームは、現在カードスロットにセットされているものと異なるウェイブフォームカードのものです。
ID Number mismatch !	同時には1つのウェイブフォームカードしか使用できないにもかかわらず、マルチを構成する各々のボイスの必要なウェイブカードが異なっているため正常に発音できません。

ディスク関係	
ディスプレイ表示	メッセージの内容
Disk not ready !	ディスクが本体に正しくセットされていません。
Illegal change !	バックアップ作業中に、新旧のディスクの順番を間違えて挿入しました。
Illegal disk !	ディスク内のデータ不良です。
Bad disk !	ディスク不良です。

File not found !	ファイルが見つかりません。
Write protected !	ディスクがプロテクトされています。
Disk full !	ディスクのメモリーが一杯です。
Directory full !	ディレクトリのエリアが一杯で、ファイルが作れません。
Media type error !	ディスクの種類が違います。
Illegal file !	本機用のファイルではありません。

シーケンサー関係	
ディスプレイ表示	メッセージの内容
Please stop sequencer !	ディスクやカードのロード、セーブまたは、バルク送信などは、シーケンサーのプレイ中には実行することはできません。
Illeagal Time !	ゲットパターンを実行しようとしたが、設定されている拍子が異なっています。
Range is exceeded !	エディットジョブで指定したパラメータは設定できる範囲を超えています。
Data not Found !	チェインパターンでサーチパートを実行したが、目的のデータはありませんでした。
Illeagal input !	エディットのインサートモードで入力しようとしたデータの値が正しくありません。
Internal buffer full !	シーケンサーを再生している時、シーケンスデータが多くて、すべてを発音することができません。(エラー処理の間、しばらくシーケンサーの発音が止まります)
Data Empty !	エディットジョブを実行しようとした小節には、データがありません。
Song Memory full !	シーケンサー用の内部メモリーが一杯です。エディットジョブの実行、MIDIの受信、ディスクのロードができません。



電池関係	
ディスプレイ表示	メッセージの内容
Change internal battery !	本体内のバックアップバッテリーが寿命です。
Change card battery !	カードのバックアップバッテリーが寿命です。
Change wave BAT ! ---	インターナル RAMまたは、増設 RAMボードのバックアップバッテリー（---の部分に表示）が寿命です。

サンプル関係	
ディスプレイ表示	メッセージの内容
Sample memory full !	サンプル領域が不足するため、データのロードができません。
Please allocate Sample memory !	サンプル領域が設定されていません。
Not enough memory for Sample !	サンプル領域が不足するため、メモリアロケートの設定を変更できません。
Sample data not exists !	指定されたサンプルナンバーにサンプルが存在しないため、バルクの送信、ディスクへのセーブ、サンプルのコピーができません。
Sample data protected !	サンプルにプロテクトがかかっているため、データのセーブ、バルク送信ができません。
Over internal waveform number !	ウェーブフォームの数が多すぎてロードできません。
Over Sample number !	サンプルの数が多すぎてロードできません。
Bulk rejected; Sample exists !	空きサンプルナンバーがないので、サンプルデータスタンダードを受信することができません。

MDR 関係	
ディスプレイ表示	メッセージの内容
MDR memory full !	MDR 領域が不足するため、データのロードができません。
Please allocate MDR memory !	MDR 領域が設定されていません。
Not enough memory for MDR !	MDR 領域が不足するため、メモリアロケートの設定を変更できません。
MDR data already exists !	既にデータが存在しているので、インプットできません。
MDR data not found !	指定された MDRナンバーにデータが存在しません。

その他	
ディスプレイ表示	メッセージの内容
Use bank D !	<ul style="list-style-type: none"> <li>・ 4 エLEMENTタイプのボイスは、バンクDにしかストアできません。</li> <li>・ Disk 1 Voice load の時、セーブ時にバンクDにあったボイスはバンクA～Cにしかロードできません。</li> </ul>
Use bank A-C !	Disk 1 Voice load の時、セーブ時にバンクA～CにあったボイスはバンクA～Cにしかロードできません。
Illegal mark !	コンペア中のため、現在の画面には、マークすることはできません。
Only C1-C6 data valid !	ドラムセットボイスをバンクA～Cにストアすると、C1～C6のデータ以外は無効となります。

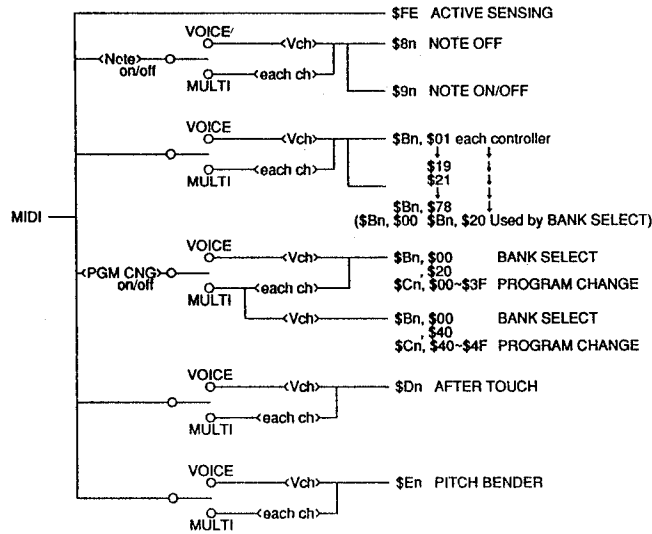
# MIDI DATA FORMAT

## 1. Synthesizer mode

### 1.1 MIDI reception/transmission block diagram

< MIDI reception conditions > 1/2

Vch ... Voice Receive ch.



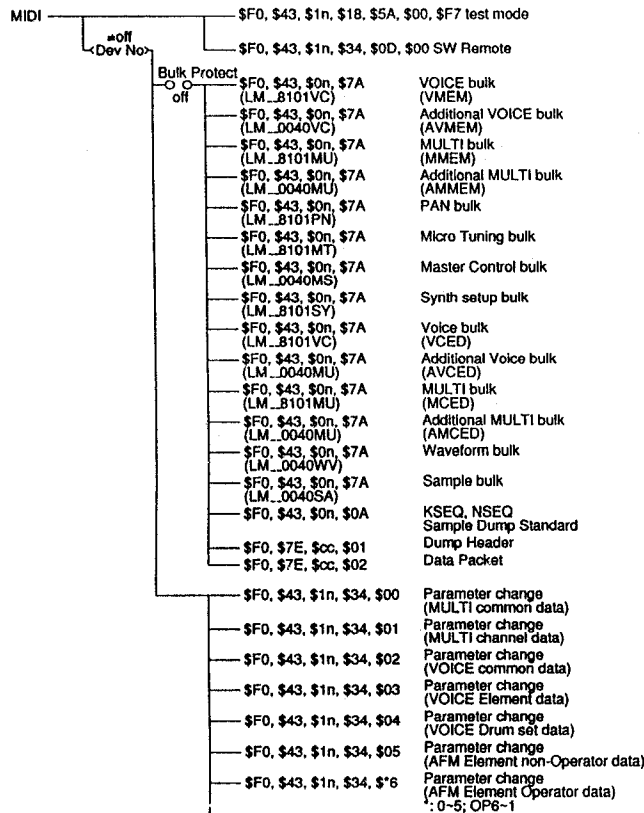
(continued on previous page)

\$F0, \$43, \$1n, \$34, \$07	Parameter change (AVM Element data)
\$F0, \$43, \$1n, \$34, \$08	Parameter change (Effector data)
\$F0, \$43, \$1n, \$34, \$09	Parameter change (Filter data)
\$F0, \$43, \$1n, \$34, \$0A	Parameter change (PAN data)
\$F0, \$43, \$1n, \$34, \$0B	Parameter change (Micro Tuning data)
\$F0, \$43, \$1n, \$34, \$0E	Parameter change (Master Control Waveform and Sample data)
\$F0, \$43, \$1n, \$34, \$0F	Parameter change (Synth System Setup data)
\$F0, \$43, \$1n, \$04, \$40	Parameter change (Master Tuning; same format as DX1)
\$F0, \$43, \$2n, \$7A (LM...B101VC)	1 VOICE bulk D.req.
\$F0, \$43, \$2n, \$7A (LM...0040VC)	1 VOICE bulk D.req. (VMEM + AVMEM)
\$F0, \$43, \$2n, \$7A (LM...B101MU)	1 MULTI bulk D.req.
\$F0, \$43, \$2n, \$7A (LM...0040MU)	1 MULTI bulk D.req. (MMEM + AMMEM)
\$F0, \$43, \$2n, \$7A (LM...B101PN)	1 PAN bulk D.req.
\$F0, \$43, \$2n, \$7A (LM...B101MT)	1 Micro Tuning bulk D.req.
\$F0, \$43, \$2n, \$7A (LM...B101SY)	System Setup bulk D.req.
\$F0, \$43, \$2n, \$7A (LM...0040WV)	1 Waveform bulk D.req.
\$F0, \$43, \$2n, \$0A	KSEQ, NSEQ bulk D.req.
\$F0, \$7E, \$cc, \$03	Sample Dump Standard
\$F0, \$7E, \$cc, \$7C	Dump Request
\$F0, \$7E, \$cc, \$7D	Wait
\$F0, \$7E, \$cc, \$7E	Cancel
\$F0, \$7E, \$cc, \$7F	NAK
	ACK

Dev No = Device Number

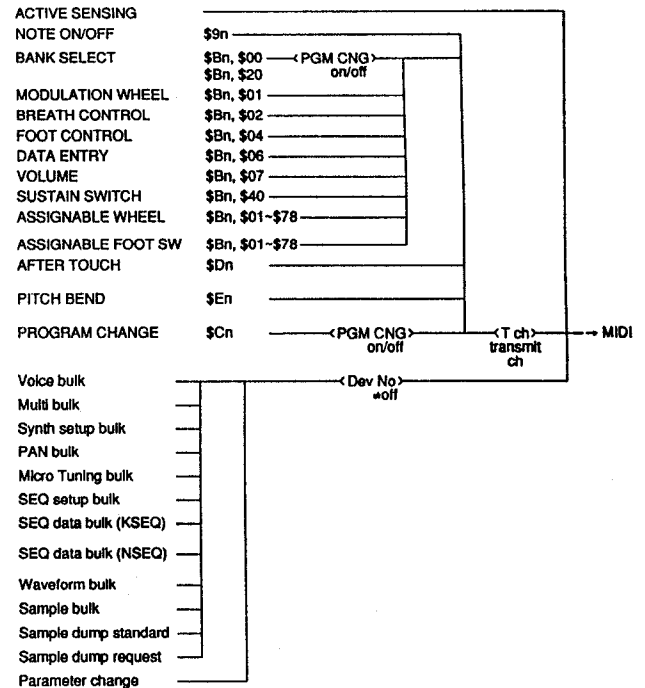
VCED = Voice edit buffer  
 AVCED = Additional Voice edit buffer  
 MCED = Multi edit buffer  
 AMCED = Additional Multi edit buffer  
 VMEM = Voice memory  
 AVMEM = Additional Voice memory  
 MMEM = Multi memory  
 AMMEM = Additional Multi memory

< MIDI reception conditions > 2/2



(continued on next page)

< MIDI transmission conditions >



## 1.2 Channel messages

### 1.2.1 Transmission

#### 1.2.1.1 Note on/off

Transmission note range = C1 (36) ... C6 (96)  
Velocity range = 0 ... 127 (0: note off)

#### 1.2.1.2 Control change

When the following controllers are moved MIDI data will be transmitted.

ctrl#	parameter	data rng
1	Modulation wheel	1~127
2	Breath control	1~127
4	Foot control	1~127
6	Data entry slider	1~127
7	Volume pedal	1~127
64	Sustain switch	1, 127
96	data increment Sw.	127
97	data decrement Sw.	127
0~120	Assignable wheel	1~127
0~120	Assignable foot sw	1, 127

← Transmitted in all modes  
other than Voice  
Play mode or Multi Play  
mode.

#### 1.2.1.3 Program change

When a voice is selected in voice mode, or when a multi is selected in multi mode, a program change is transmitted. The program change number is assigned according to the mode, as follows.

		Bank No. (MSB), (LSB)	PGM CNG No.
Voice	Internal	1 (\$00), (\$00)	1~64 (\$00~\$3F)
	Card	2 (\$00), (\$01)	↓
	Preset 1	3 (\$00), (\$02)	↓
	Preset 2	6 (\$00), (\$05)	↓
Multi	Internal	17 (\$00), (\$10)	65~80 (\$40~\$4F)
	Card	18 (\$00), (\$11)	↓
	Preset	19 (\$00), (\$12)	↓
Voice in Multi	Internal	33 (\$00), (\$20)	1~64 (\$00~\$3F)
	Card	34 (\$00), (\$21)	↓
	Preset 1	35 (\$00), (\$22)	↓
	Preset 2	38 (\$00), (\$25)	↓

BANK SELECT      \$Bn, \$00, \$00~\$7F (MSB)  
                              \$Bn, \$20, \$00~\$7F (LSB)  
PROGRAM CHANGE    \$Cn, \$00~\$7F

No bank select or program change messages are transmitted if Program Change mode is set to OFF.

#### 1.2.1.4 Pitch bend

Pitch bend is transmitted with 7 bit precision.

#### 1.2.1.5 Aftertouch

Transmitted from MIDI when aftertouch is operated.

#### 1.2.1.6 Channel mode messages

Channel mode messages are not transmitted.

## 1.2.2 Reception

### 1.2.2.1 Note on/off

Received note range = C-2 ... G8  
Velocity range = 1 ... 127 (note on only)

\* A system setup parameter allows selection of  
normal = receive all note numbers  
odd = receive odd note numbers  
even = receive even note numbers

### 1.2.2.2 Control change

The following parameters can be controlled via MIDI.

cntrl#	parameter	data rng
1~120	Pitch Modulation	0...127
1~120	Amplitude Modulation	0...127
1~120	Filter Modulation	0...127
1~120	Pan LFO Modulation	0...127
1~120	Cutoff Bias	0...127
1~120	Pan Bias	0...127
1~120	EG Bias	0...127
1~120	Volume (assignable)	0...127
5	Portamento Time	0...127
7	Volume	0...127
64	Sustain Switch	0...127
65	Portamento Switch	0...127

Control #s 0(\$00) and 32(\$20) are used for bank select.

### 1.2.2.3 Program change

The SY99 responds as follows when a program change message is received:

- 1) If Program Change mode is OFF:  
: Bank select and program change messages are not recognized.
- 2) If Program Change mode is ON:  
: Response as described by the chart in 2.2.1.3. Voice selection is carried out upon reception of the program change message.

### 1.2.2.4 Pitch bend

Pitch bend is recognized by the MSB only.

### 1.2.2.5 Aftertouch

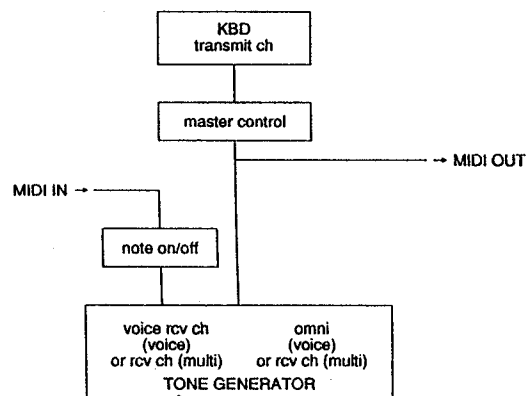
Channel aftertouch is recognized. Polyphonic aftertouch is not recognized.

### 1.2.2.6 Channel mode messages

Not received

## 1.2.3 Diagram of the keyboard section and tone generator section

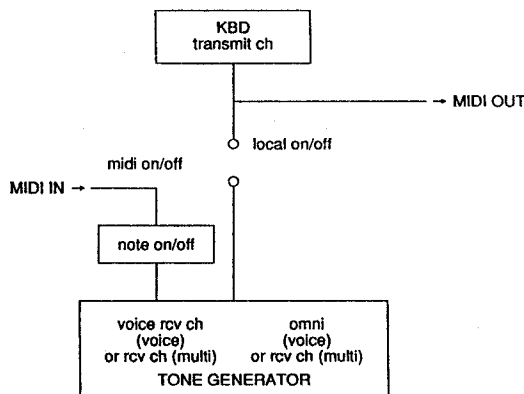
\* Normal mode



Note 1) In voice mode, sound will be produced even if the Voice Receive Channel does not match the Keyboard Trans. Channel.

Note 2) Notes from the keyboard and notes from MIDI will be distinguished in polyphonic mode, and not distinguished in monophonic mode. Controller data from the keyboard and controller data from the MIDI (control change, aftertouch, pitch bend) will not be distinguished except for the sustain switch.

## \* Master control mode



## 2. System exclusive messages

## 2.1 Parameter changes

The SY99 is capable of transmitting and recognizing the following 17 types of parameter change message (with the exception of 14. Switch Remote, which is recognized but cannot be transmitted). Recognition of 14. Switch Remote has the same effect on the display as pressing the switch.

- 1). Multi Common Data parameter change
- 2). Multi Channel Data parameter change
- 3). Voice Common Data parameter change
- 4). Voice Element Data parameter change
- 5). Voice Drum Set Data parameter change
- 6). AFM Element Common Data parameter change
- 7). AFM Element Operator Data parameter change
- 8). AWM Element Data parameter change
- 9). Waveform Data parameter change
- 10). Effect Data parameter change
- 11). Filter Data parameter change
- 12). PAN Data parameter change
- 13). Micro Tuning Data parameter change
- 14). Switch Remote parameter change
- 15). Master Control Data parameter change
- 16). System Setup Data parameter change
- 17). Sample Data parameter change

Parameter message recognition can be turned off by turning the Device Number switch off. It cannot be turned off using any other MIDI switch.

## 2.1.1 Multi Common Data parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00000000 00
00000000 00
00000000 00
00000000 00
000ppppp ppppp - Table 1-1, N2
00000000 00
0vvvvvvv vvvvvvv - ascl1
11110111 F7

```

This message modifies Multi Common data (multi name) one parameter at a time. When this message is received, the following will occur.

Voice Play mode : ignore.  
 Voice Edit mode : ignore.  
 Multi Play mode : move to Multi Edit mode and receive. (Display changes.)  
 Multi Edit mode : receive. (Display changes.)  
 Voice Edit mode in Multi : receive.  
 Utility mode (Voice mode) : ignore.  
 Utility mode (Multi mode) : move to Voice Edit mode and receive. (Display changes.)

## 2.1.2 Multi Channel Data parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00000001 01
0000cccc cccc - Voice Channel Number
00000000 00
000ppppp ppppp - Table 1-2, N2
00000000 00
0vvvvvvv vvvvvvv - Data Value
11110111 F7

```

This message modifies the channel data of a multi one parameter at a time. When this message is received, the following will occur.

Voice Play mode : ignore.  
 Voice Edit mode : ignore.  
 Multi Play mode : move to Multi Edit mode and receive. (Display changes.)  
 Multi Edit mode : receive. (Display changes.)  
 Voice Edit mode in Multi : receive.  
 Utility mode (Voice mode) : ignore.  
 Utility mode (Multi mode) : move to Voice Edit mode and receive. (Display changes.)

## 2.1.3 Voice Common Data parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00000010 02
00000000 00
00000000 00
0ppppppp ppppppp - Table 1-3, N2
00000000 00
0vvvvvvv vvvvvvv - Data Value
11110111 F7

```

This message modifies voice common data one parameter at a time. When this message is received, the following will occur.

Voice Play mode : move to Voice Edit mode and receive. (Display changes.)  
 Voice Edit mode : receive. (Display changes.)  
 Multi Play mode : ignore.  
 Multi Edit mode : ignore.  
 Voice Edit mode in Multi : receive. (Display changes.)  
 Utility mode (Voice mode) : move to Voice Edit mode and receive. (Display changes.)  
 Utility mode (Multi mode) : ignore.

## 2.1.4 Voice Element Data parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00000011 03
0ee00000 ee - Element Number
00000000 00
0000pppp pppp - Table 1-4, N2
00000000 00
0vvvvvvv vvvvvvv - Data Value
11110111 F7

```

This message modifies voice element data one parameter at a time. When this message is received, the following will occur.

Voice Play mode : if the specified element exists, move to Voice Edit mode and receive. If not, ignore.  
 Voice Edit mode : if the specified element exists, receive. If not, ignore. (The screen goes into Edit Mode.)  
 Multi Play mode : ignore.  
 Multi Edit mode : ignore.  
 Voice Edit mode in Multi : same as for Voice Edit mode.  
 Utility mode (Voice mode) : same as for Voice Play mode.  
 Utility mode (Multi mode) : ignore.



## 2.1.5 Voice Drum Set Data parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00000100 04
0mmmmmmmm mmmmmmm - MIDI Note Number
00000000 00
0000pppp pppp - Table 1-5, N2
0000000v v - Data Value (MSB)
0vvvvvvv vvvvvv - Data Value (LS7bits)
11110111 F7

```

This message modifies voice drum set data one parameter at a time. When this message is received, the following will occur.

**Voice Play mode** : if originally a drum set, move to Voice Edit mode and receive. (Display changes.) If not, ignore. (The screen goes into Edit Mode.)

**Voice Edit mode** : if originally a drum set, receive. (Display changes.) If not, ignore.

**Multi Play mode** : ignore.

**Multi Edit mode** : ignore.

**Voice Edit mode in Multi** : same as for Voice Edit mode.

**Utility mode (Voice mode)** : same as for Voice Play mode.

**Utility mode (Multi mode)** : ignore.

## 2.1.6 AFM Element Common Data parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00000101 05
0ee00000 ee - Element Number
00000000 00
000ppppp pppp - Table 1-6, N2
00000000 00
0vvvvvvv vvvvvv - Data Value
11110111 F7

```

This message modifies AFM element common data one parameter at a time. When this message is received, the following will occur.

**Voice Play mode** : if the specified element exists and is AFM, move to Voice Edit mode and receive. (Display changes.) If not, ignore. (The screen goes into Edit Mode.)

**Voice Edit mode** : if the specified element exists and is AFM, receive. If not, ignore. (Display changes.)

**Multi Play mode** : ignore.

**Multi Edit mode** : ignore.

**Voice Edit mode in Multi** : same as Voice Edit mode.

**Utility mode (Voice mode)** : same as Voice Play mode.

**Utility mode (Multi mode)** : ignore.

## 2.1.7 AFM Element Operator Enable Parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00000101 05
0ee00000 ee - Element Number
01111111 7F
01111111 7F
00000000 00
0vvvvvvv vvvvvv - Data Value
11110111 F7

```

This message modifies AFM operator enable data one parameter at a time. When this message is received, the following will occur.

**Voice Play mode** : if the specified element exists and is AFM, move to Voice Edit mode and receive. (Display changes.) If not, ignore. (The screen goes into Edit Mode.)

**Voice Edit mode** : if the specified element exists and is AFM, receive. If not, ignore. (Display changes.)

**Multi Play mode** : ignore.

**Multi Edit mode** : ignore.

**Voice Edit mode in Multi** : same as Voice Edit mode.

**Utility mode (Voice mode)** : same as Voice Play mode.

**Utility mode (Multi mode)** : ignore.

## 2.1.8 AFM Element Operator Data Parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
0ooo0110 ooo - 6 (Operator Number)
0ee00000 ee - Element Number
00000000 00
0ppppppp pppppp - Table 1-7, N2
0000000v v - Data Value (MSB)
0vvvvvvv vvvvvv - Data Value (LS7bits)
11110111 F7

```

This message modifies AFM operator parameter data one parameter at a time. When this message is received, the following will occur.

**Voice Play mode** : if the specified element exists and is AFM, move to Voice Edit mode and receive. (Display changes.) If not, ignore. (The screen goes into Edit Mode.)

**Voice Edit mode** : if the specified element exists and is AFM, receive. (Display changes.) If not, ignore.

**Multi Play mode** : ignore.

**Multi Edit mode** : ignore.

**Voice Edit mode in Multi** : same as in Voice Edit mode.

**Utility mode (Voice mode)** : same as in Voice Play mode.

**Utility mode (Multi mode)** : ignore.

## 2.1.9 AWM Element Data parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00000111 07
0ee00000 ee - Element Number
00000000 00
0ppppppp pppppp - Table 1-8, N2
0000000v v - Data Value (MSB)
0vvvvvvv vvvvvv - Data Value (LS7bits)
11110111 F7

```

This message modifies AWM element data one parameter at a time. When this message is received, the following will occur.

**Voice Play mode** : if the specified element exists and is AWM, move to Voice Edit mode and receive. (Display changes.) If not, ignore. (The screen goes into Edit Mode.)

**Voice Edit mode** : if the specified element exists and is AWM, receive. If not, ignore. (Display changes.)

**Multi Play mode** : ignore.

**Multi Edit mode** : ignore.

**Voice Edit mode in Multi** : same as in Voice Edit mode.

**Utility mode (Voice mode)** : same as in Voice Play mode.

**Utility mode (Multi mode)** : ignore.

## 2.1.10 Waveform and Sample parameter change

## Waveform parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00001110 0E
00wwwww wwwwww - Waveform Number
00000101 05
0ppppppp pppppp - Table 1-9, N2
00000000 00
0vvvvvvv vvvvvv - Data Value
11110111 F7

```

## Sample parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00001110 0E
0sssssss ssssss - Sample Number
00000101 06
0ppppppp pppppp - Table 1-17, N2
00000000 00
0vvvvvvv vvvvvv - Data Value
11110111 F7

```

These messages change a single parameter of waveform or sample data. These messages are recognized, and the data for the specified waveform or sample are changed, regardless of the SY99's current mode setting.

### 2.1.11 Effect Data parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00001000 08
00000000 00
00000000 00
000ppppp ppppp - Table 1-10, N2
00000000 00
0vvvvvvv vvvvvv - Data Value
11110111 F7

```

This message modifies effect data one parameter at a time. When this message is received, the following will occur.

Voice Play mode : move to Voice Edit mode and receive.  
 Voice Edit mode : receive. (Display changes.)  
 Multi Play mode : move to Multi Edit mode and receive.  
 Multi Edit mode : receive. (Display changes.)  
 Voice Edit mode in Multi : receive. Modify the Multi effect. (Display changes.)  
 Utility mode (Voice mode) : same as in Voice Play mode.  
 Utility mode (Multi mode) : same as in Multi Play mode.

### 2.1.12 Filter Data parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00001001 09
0ee0ffff ee - Element Number, fff - filter Number
00000000 00
0ppppppp pppppp - Table 1-11, N2
0000000v v - Data Value (MSB)
0vvvvvvv vvvvvv - Data Value (LS7bits)
11110111 F7

```

This message modifies filter data one parameter at a time. When this message is received, the following will occur.

Voice Play mode : if the specified element exists, move to Voice Edit mode and receive. If not, ignore.  
 Voice Edit mode : if the specified element exist, receive. If not, ignore. (Display changes.)  
 Multi Play mode : ignore.  
 Multi Edit mode : ignore.  
 Voice Edit mode in Multi : same as in Voice Edit mode.  
 Utility mode (Voice mode) : same as in Voice Play mode.  
 Utility mode (Multi mode) : ignore.

### 2.1.13 PAN Data parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00001010 0A
000mmmmmm mmmmm - Memory Number
00000000 00
000ppppp ppppp - Table 1-12, N2
00000000 00
0vvvvvvv vvvvvv - Data Value
11110111 F7

```

This message modifies dynamic pan data one parameter at a time. When this message is received, the mode will not change, and the pan data of the specified memory will be modified.

### 2.1.14 Micro Tuning Data parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00001010 0B
000mmmmmm mmmmm - Memory Number
0000000p p - Table 1-13, N1
0ppppppp pppppp - Table 1-13, N2
0vvvvvvv vvvvvv - Data Value (MS7bits)
0vvvvvvv vvvvvv - Data Value (LS7bits)
11110111 F7

```

This message modifies micro tuning data one parameter at a time. When this message is received, the mode will not change, and the micro tuning data of the specified memory will be modified.

### 2.1.15 Switch Remote parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00001010 00
00000000 00
00000000 00
0ppppppp pppppp - Table 1-14, N2
00000000 00
0vvvvvvv vvvvvv - Data Value
11110111 F7

```

This message is only received, and allows remote control of all panel switches. The message will have the same effect as if that switch had been pressed.

### 2.1.16 Master Control Data parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00001110 0E
00nn0ttt ntttt - Table 1-15, T2
0ppppppp pppppp - Table 1-15, N1
0ppppppp pppppp - Table 1-15, N2
0vvvvvvv vvvvvv - Data Value
0vvvvvvv vvvvvv - Data Value
11110111 F7

```

This message modifies master control data one parameter at a time. When this message is received, the mode will not change.

### 2.1.17 System Setup Data parameter change

```

11110000 F0
01000011 43
0001nnnn nnnn - Device Number
00110100 34
00001111 0F
00000000 00
00000000 00
0ppppppp pppppp - Table 1-16, N2
00000000 00
0vvvvvvv vvvvvv - Data Value
11110111 F7

```

This message modifies system setup data one parameter at a time. When this message is received, the mode will not change.

## 3. Bulk dump

Reception is possible any time when not playing back or recording. The data is transmitted when the MIDI UTILITY "bulk dump" is executed or when a dump request is received.

### 3.1 Voice data bulk dump

There are nine types of voice data bulk dump as follows.

- 1AFM Voice bulk dump
- 2AFM Voice bulk dump
- 4AFM Voice bulk dump
- 1AWM Voice bulk dump
- 2AWM Voice bulk dump
- 4AWM Voice bulk dump
- 1AFM\_1AWM Voice bulk dump
- 2AFM\_2AWM Voice bulk dump
- Drum\_set Voice bulk dump

```

0 11110000 F0
1 01000011 43
2 0000nnnn nnnn - Device Number
3 01110100 7A
4 0bbbbb b byte count
5 0bbbbb b
6 01001100 4C(ascii"L")
7 01001101 4D(ascii"M")
8 00100000 20(ascii" ")
9 00100000 20(ascii" ")
10 00111000 38(ascii"8")
11 00110001 31(ascii"1")
12 00110000 30(ascii"0")
13 00110001 31(ascii"1")
14 01010110 56(ascii"V")
15 01000011 43(ascii"C")
16 00000000 00
↓
29 00000000 00
30 0tttttt tttttt - Memory_type
31 00mmmmmm mmmmm - Memory Number
32 0ddddd dddddd - data
↓
0sssssss ssssss - check_sum
11110111 F7

```

**MIDI Utility 1 Voice Bulk transmission**

Memory\_type = 7F  
Memory Number = 00

**MIDI Utility Vc & Mlt Bulk or 64 Voices Bulk transmission**

Memory\_type = 00 (INT)  
Memory Number = start from 0 and transmit consecutively to 63 (During Vc & Mlt, start from Multi 0 and transmit consecutively to 15.)

**1 Voice Bulk transmission by Dump Request**

Memory\_type = 00 (INT)  
02 (PRESET1)  
03 (PRESET2)  
7F (Edit\_Buffer)  
Memory Number = 0-63 (the number specified by the Dump Request)

For reception, data will be processed as Edit\_buffer when the Memory\_type is 7F, and as INTERNAL for other cases.

\* For details of the bulk dump data and dump request format, refer to table 2-1.

For transmission at the main unit panel operation, additional voice data is also transmitted. When a dump request is received, only voice data is transmitted.

**3.2 Additional voice data bulk dump**

- 1). 1AFM & 1AWM Voice bulk dump
- 2). 2AFM & 2AWM & 1AFM\_1AWM Voice bulk dump
- 3). 4AFM & 4AWM & 2AFM\_2AWM Voice bulk dump
- 4). Drum\_set Voice bulk dump

```

0 11110000 F0
1 01000011 43
2 0000nnnn nnnn - Device Number
3 01111010 7A
4 0bbbbbbb ] byte count
5 0bbbbbbb
6 01001100 4C(ascii"L")
7 01001101 4D(ascii"M")
8 00100000 20(ascii" ")
9 00100000 20(ascii" ")
10 00110000 30(ascii"0")
11 00110000 30(ascii"0")
12 00110100 34(ascii"4")
13 00110000 30(ascii"0")
14 01010110 56(ascii"V")
15 01000011 43(ascii"C")
16 00000000 00
↓
29 00000000 00
30 0ttttttt tttttt - Memory_type
31 00mmmmmm mmmmmm - Memory Number
32 0ddddd dddddd - data
↓
0sssssss ssssss - check_sum
11110111 F7

```

**MIDI Utility 1 Voice Bulk transmission**

Memory\_Type = 7F  
Memory Number = 00

**MIDI Utility Vc & Mlt Bulk or 64 Voice Bulk transmission**

Memory\_type = 00 (INT)  
Memory Number = start from 0 and transmit consecutively to 63 (During Vc & Mlt, start from Multi 0 and transmit consecutively to 15.)

**1 Voice Bulk transmission by Dump Request**

Memory\_type = 00 (INT)  
02 (PRESET1)  
03 (PRESET2)  
Memory Number = 0-63 (the number specified by the Dump Request)

For reception, data will be processed as Edit\_buffer when the Memory\_type is 7F, and as INTERNAL for other cases.

\* For details of the bulk dump data and dump request format, refer to table 2-2.

For transmission at the main unit panel operation or at the reception of a dump request, voice data is also transmitted.

**3.3 Multi data bulk dump**

```

0 11110000 F0
1 01000011 43
2 0000nnnn nnnn - Device Number
3 01111010 7A
4 0bbbbbbb ] byte count
5 0bbbbbbb
6 01001100 4C(ascii"L")
7 01001101 4D(ascii"M")
8 00100000 20(ascii" ")
9 00100000 20(ascii" ")
10 00110000 38(ascii"8")
11 00110001 31(ascii"1")
12 00110000 30(ascii"0")
13 00110001 31(ascii"1")
14 01001101 4D(ascii"M")
15 01010101 55(ascii"U")
16 00000000 00
↓
29 00000000 00
30 0ttttttt tttttt - Memory_type
31 00mmmmmm mmmmmm - Memory Number
32 0ddddd dddddd - data
↓
0sssssss ssssss - check_sum
11110111 F7

```

**MIDI Utility 1 Multi Bulk transmission**

Memory\_type = 7F  
Memory Number = 00

**MIDI Utility Vc & Mlt Bulk or 16 Multi Bulk transmission**

Memory\_type = 00 (INT)  
Memory Number = start from 0 and transmit consecutively to 15 (During Vc & Mlt, start from Voice 0 and transmit consecutively to 63.)

**1 Multi Bulk transmission by Dump Request**

Memory\_type = 00 (INT)  
02 (PRESET)  
Memory Number = 0-15 (the number specified by the Dump Request)

For reception, data will be processed as Edit\_buffer when the Memory\_type is 7F, and as INTERNAL for other cases.

\* For details of the bulk dump data and dump request format, refer to table 3-1.

For transmission at the main unit panel operation, additional voice data is also transmitted. When a dump request is received, only multi data is transmitted.

**3.4 Additional multi data bulk dump**

```

0 11110000 F0
1 01000011 43
2 0000nnnn nnnn - Device Number
3 01111010 7A
4 0bbbbbbb ] byte count
5 0bbbbbbb
6 01001100 4C(ascii"L")
7 01001101 4D(ascii"M")
8 00100000 20(ascii" ")
9 00100000 20(ascii" ")
10 00110000 30(ascii"0")
11 00110000 30(ascii"0")
12 00110100 34(ascii"4")
13 00110000 30(ascii"0")
14 01001101 4D(ascii"M")
15 01010101 55(ascii"U")
16 00000000 00
↓
29 00000000 00
30 0ttttttt tttttt - Memory_type
31 00mmmmmm mmmmmm - Memory Number
32 0ddddd dddddd - data
↓
0sssssss ssssss - check_sum
11110111 F7

```

**MIDI Utility 1 Multi Bulk transmission**

Memory\_type = 7F  
Memory Number = 00

## MIDI Utility Vc &amp; Mlt Bulk or 16 Multi Bulk transmission

Memory\_type = 00 (INT)  
 Memory Number = start from 0 and transmit consecutively to 15. (During Vc & Mlt, start from Voice 0 and transmit consecutively to 63.)

## 1 Multi Bulk transmission by Dump Request

Memory\_type = 00 (INT) 02 (PRESET)  
 Memory Number = 0~15 (the number specified by the Dump Request)

For reception, data will be processed as Edit\_buffer when the Memory\_type is 7F, and as INTERNAL for other cases.

\* For details of the bulk dump data and dump request format, refer to table 3-2.

For transmission at the main unit panel operation or at the reception of a dump request, voice data is also transmitted.

## 3.5 Pan data bulk dump

```

0  11110000  F0
1  01000011  43
2  0000nnnn  nnnn - Device Number
3  01111010  7A
4  0bbbbbbb  byte count
5  0bbbbbbb
6  01001100  4C(ascii"L")
7  01001101  4D(ascii"M")
8  00100000  20(ascii" ")
9  00100000  20(ascii" ")
10 00111000  38(ascii"8")
11 00110001  31(ascii"1")
12 00110000  30(ascii"0")
13 00110001  31(ascii"1")
14 01010000  50(ascii"P")
15 01001110  4E(ascii"N")
16 00000000  00
↓
29 00000000  00
30 0ttttttt  tttttt - Memory_type
31 00mmmmmm  mmmmmm - Memory Number
32 0ddddd  dddddd - data
↓
0sssssss  ssssss - check_sum
11110111  F7
  
```

## MIDI Utility Vc &amp; Mlt Bulk or PAN Bulk transmission

Memory\_type = 00 (INT)  
 Memory Number = start from 0 and transmit consecutively to 31

## PAN Bulk transmission by Dump Request

Memory\_type = 00 (INT) 02 (PRESET)  
 Memory Number = 0~63 (the number specified by the Dump Request)

For reception, bits 5 and 6 of Memory\_type and memory Number will be ignored, and the data will be processed as INTERNAL.

\* For details of the bulk dump data and dump request format, refer to table 4.

## 3.6 Micro tuning data bulk dump

```

0  11110000  F0
1  01000011  43
2  0000nnnn  nnnn - Device Number
3  01111010  7A
4  0bbbbbbb  byte count
5  0bbbbbbb
6  01001100  4C(ascii"L")
7  01001101  4D(ascii"M")
8  00100000  20(ascii" ")
9  00100000  20(ascii" ")
10 00111000  38(ascii"8")
11 00110001  31(ascii"1")
12 00110000  30(ascii"0")
13 00110001  31(ascii"1")
14 01001101  4D(ascii"M")
15 01010100  54(ascii"T")
16 00000000  00
↓
29 00000000  00
30 00000000  00 - Memory_type
31 00mmmmmm  mmmmmm - Memory Number
32 0ddddd  dddddd - data
↓
0sssssss  ssssss - check_sum
11110111  F7
  
```

## MIDI Utility Vc &amp; Mlt Bulk or Micro Tuning Bulk transmission

Memory\_type = 00 (INT)  
 Memory Number = start from 0 and transmit consecutively to 1

## MCT Bulk transmission by Dump Request

Memory\_type = 00 (INT) 02 (PRESET)  
 Memory Number = 0~63 (the number specified by the Dump Request)

For reception, bits 1~6 of Memory\_type and Memory Number will be ignored, and the data will be processed as INTERNAL.

\* For details of the bulk dump data and dump request format, refer to table 5.

## 3.7 Master control data bulk dump

```

0  11110000  F0
1  01000011  43
2  0000nnnn  nnnn - Device Number
3  01111010  7A
4  0bbbbbbb  byte count
5  0bbbbbbb
6  01001100  4C(ascii"L")
7  01001101  4D(ascii"M")
8  00100000  20(ascii" ")
9  00100000  20(ascii" ")
10 00111000  38(ascii"8")
11 00110001  31(ascii"1")
12 00110000  30(ascii"0")
13 00110001  31(ascii"1")
14 01001101  4D(ascii"M")
15 01010011  53(ascii"S")
16 00000000  00
↓
31 00000000  00
32 0ddddd  dddddd - data
↓
0sssssss  ssssss - check_sum
11110111  F7
  
```

\* For details of the bulk dump data and dump request format, refer to table 6.

Data transmitted at the main unit panel operation is followed by SYNTH system setup data when it is transmitted.

For transmission at the reception of a dump request, only master control data is transmitted.

## 3.8 SYNTH system setup data bulk dump

```

0  11110000  F0
1  01000011  43
2  0000nnnn  nnnn - Device Number
3  01111010  7A
4  0bbbbbbb  byte count
5  0bbbbbbb
6  01001100  4C(ascii"L")
7  01001101  4D(ascii"M")
8  00100000  20(ascii" ")
9  00100000  20(ascii" ")
10 00111000  38(ascii"8")
11 00110001  31(ascii"1")
12 00110000  30(ascii"0")
13 00110001  31(ascii"1")
14 01010011  53(ascii"S")
15 01010011  59(ascii"Y")
16 00000000  00
↓
31 00000000  00
32 0ddddd  dddddd - data
↓
0sssssss  ssssss - check_sum
11110111  F7
  
```

\* For details of the bulk dump data and dump request format, refer to table 7.

For transmission at the main unit panel operation, master control data is transmitted before this data.

For transmission at the reception of a dump request, only this data is transmitted.

## 3.9 SEQ setup data bulk dump

```

0 11110000 F0
1 01000011 43
2 0000nnnn nnnn - Device Number
3 01111110 7E
4 0bbbbbbb byte count
5 0bbbbbbb
6 01001100 4C(ascii"L")
7 01001101 4D(ascii"M")
8 00100000 20(ascii" ")
9 00100000 20(ascii" ")
10 00111000 38(ascii"8")
11 00110001 31(ascii"1")
12 00110000 30(ascii"0")
13 00110001 31(ascii"1")
14 01010011 53(ascii"S")
15 01010011 53(ascii"S")
16 0ddddddd ddddddd - data
↓
0sssssss sssssss - check_sum
11110111 F7

```

\* For details of the bulk dump data, refer to table 8-1.

## Dump request

```

0 11110000 F0
1 01000011 43
2 0000nnnn nnnn - Device Number
3 01111110 7E
4 01001100 4C(ascii"L")
5 01001101 4D(ascii"M")
6 00100000 20(ascii" ")
7 00100000 20(ascii" ")
8 00111000 38(ascii"8")
9 00110001 31(ascii"1")
10 00110000 30(ascii"0")
11 00110001 31(ascii"1")
12 01010011 53(ascii"S")
13 01010011 53(ascii"S")
14 11110111 F7

```

## 3.10 SEQ song and pattern data bulk dump (KSEQ)

Reception is possible at any time when not playing or recording. This data is transmitted when the MIDI UTILITY "bulk dump" is executed, or when a dump request is received.

```

0 11110000 F0
1 01000011 43
2 0000nnnn nnnn - Device Number
3 00001010 0A
4 0bbbbbbb byte count
5 0bbbbbbb max. 4096
6 01001100 4C(ascii"L")
7 01001101 4D(ascii"M")
8 00100000 20(ascii" ")
9 00100000 20(ascii" ")
10 01001011 4E(ascii"N")
11 01010011 53(ascii"S")
12 01000101 45(ascii"E")
13 01010010 51(ascii"O")
14 00100000 20(ascii" ")
15 00100000 20(ascii" ")
16 0ddddddd ddddddd - data
↓
0sssssss sssssss - check_sum
11110111 F7

```

When the byte count is below 4096, the byte count is that count. When the byte count exceeds 4096, a byte count and check\_sum operation is repeated for every 4096 bytes marked off from the top.

## Dump request

```

0 11110000 F0
1 01000011 43
2 0000nnnn nnnn - Device Number
3 00001010 0A
4 01001100 4C(ascii"L")
5 01001101 4D(ascii"M")
6 00100000 20(ascii" ")
7 00100000 20(ascii" ")
8 01001011 4E(ascii"N")
9 01010011 53(ascii"S")
10 01000101 45(ascii"E")
11 01010010 51(ascii"O")
12 00100000 20(ascii" ")
13 00100000 20(ascii" ")
14 11110111 F7

```

## 3.11 SEQ song and pattern data bulk dump (NSEQ)

Reception is possible at any time when not playing or recording. This data is transmitted when the MIDI UTILITY "bulk dump" is executed, or when a dump request is received.

```

0 11110000 F0
1 01000011 43
2 0000nnnn nnnn - Device Number
3 00001010 0A
4 0bbbbbbb byte count
5 0bbbbbbb max. 4096
6 01001100 4C(ascii"L")
7 01001101 4D(ascii"M")
8 00100000 20(ascii" ")
9 00100000 20(ascii" ")
10 01001110 4E(ascii"N")
11 01010011 53(ascii"S")
12 01000101 45(ascii"E")
13 01010010 51(ascii"O")
14 00100000 20(ascii" ")
15 00100000 20(ascii" ")
16 0ddddddd ddddddd - data
↓
0sssssss sssssss - check_sum
11110111 F7

```

When the byte count is below 4096, the byte count is that count. When the byte count exceeds 4096, a byte count and check\_sum operation is repeated for every 4096 bytes marked off from the top.

## Dump request

```

0 11110000 F0
1 01000011 43
2 0000nnnn nnnn - Device Number
3 00001010 0A
4 01001100 4C(ascii"L")
5 01001101 4D(ascii"M")
6 00100000 20(ascii" ")
7 00100000 20(ascii" ")
8 01001110 4E(ascii"N")
9 01010011 53(ascii"S")
10 01000101 45(ascii"E")
11 01010010 51(ascii"O")
12 00100000 20(ascii" ")
13 00100000 20(ascii" ")
14 11110111 F7

```

## 3.12 Waveform data bulk dump

```

0 11110000 F0
1 01000011 43
2 0000nnnn nnnn - Device Number
3 01111010 7A
4 0bbbbbbb byte count
5 0bbbbbbb
6 01001100 4C(ascii"L")
7 01001101 4D(ascii"M")
8 00100000 20(ascii" ")
9 00100000 20(ascii" ")
10 00110000 30(ascii"0")
11 00110000 30(ascii"0")
12 00110100 34(ascii"4")
13 00110000 30(ascii"0")
14 01010111 57(ascii"W")
15 01010110 56(ascii"V")
16 00000000 00
↓
29 00000000 00
30 00000ttt ttt - Memory_type
31 0mmmmmmmm mmmmmmm - Memory Number
32 0ddddddd ddddddd - data
↓
0sssssss sssssss - check_sum
11110111 F7

```

## Dump request

```

0 11110000 F0
1 01000011 43
2 0010nnnn nnnn - Device Number
3 01111010 7A
4 01001100 4C(ascii"L")
5 01001101 4D(ascii"M")
6 00100000 20(ascii" ")
7 00100000 20(ascii" ")
8 00110000 30(ascii"0")
9 00110000 30(ascii"0")
10 00110100 34(ascii"4")
11 00110000 30(ascii"0")
12 01010111 57(ascii"W")
13 01010110 56(ascii"V")
14 00000000 00
↓
27 00000000 00
28 00000ttt ttt - Memory_type
29 0mmmmmmmm mmmmmmm - Memory Number
30 11110111 F7

```

The Sample utility Waveform Bulk Dump operation transmits the following information:

Memory\_type = \$00 (INT)  
Memory number = \$00 to \$3F, in sequence



A bulk dump in response to a dump request message transmits the following:

Memory\_type = \$00 (INT), \$01 (CARD), \$02, \$03 (PRE1), \$04 (PRE2)  
Memory number = a number from \$00 to \$3F, as specified by the dump request

	Preset 1, numbers 1 to 128	Preset 1, numbers 129 to 155
Memory_type	\$02	\$03
Memory Number	\$00-\$7F	\$00-\$1A

Requests for nonexistent numbers are ignored.

Incoming bulk dumps are handled as INTERNAL memory; bit 6 of Memory\_type and Memory Number are ignored.

\* Refer to attached Table 9-1 for details regarding bulk dump data format.

#### 4. Sample dumps

The SY99 is capable of handling two sample dumps in two formats: the Sample Dump Standard, and the SY99 Sample Bulk Dump. Sample dumps in both of these formats are recognized. Sample dumps in both are transmitted when the Sample utility Sample Dump operation is executed, and in response to a Sample Dump Standard Dump Request. When an SY99 Sample Bulk Dump Request is received, the SY99 Sample Bulk Dump only is transmitted. The upper limit on sample numbers for dumps in either format is set at \$62; sample numbers higher than \$62 are treated as \$62.

##### Sample Dump Standard

```
DUMP REQ  F0. 7E. cc. 03. ss. $$. F7
ACK       F0. 7E. cc. 7E. dd. F7
NAK       F0. 7E. cc. 7E. dd. F7
CANCEL    F0. 7E. cc. 70. dd. F7
WAIT      F0. 7E. cc. 70. dd. F7
DATA PACKET F0. 7E. cc. 02. kk. <120 byte>. 11. F7
DUMP HEADER F0. 7E. cc. 01. ss. ee. ff. ff. gg. gg. gg. gg.
           hh. hh. hh. ii. ii. ii. jj. F7
```

pp : packet number  
cc : channel number  
ss ss : sample number  
ee : sample format (8 to 28 bits; SY99 handles samples of 16 bits or less)  
ff ff ff : sample period  
gg gg gg : sample length  
hh hh hh : loop start  
ii ii ii : loop end  
jj : loop type  
kk : running packet count (0-127)  
          (number of current packet)  
11 : checksum (XOR of 7E cc 02 kk <120 bytes>)

##### SY99 Sample Bulk Dump

```
0 11110000 F0
1 01000011 43
2 0000nnnn nnnn - Device Number
3 01111010 7A
4 0bbbbbbb byte count
5 0bbbbbbb
6 01001100 4C(ascii"L")
7 01001101 4D(ascii"M")
8 00100000 20(ascii" ")
9 00100000 20(ascii" ")
10 00110000 30(ascii"0")
11 00110000 30(ascii"0")
12 00110100 34(ascii"4")
13 00110000 30(ascii"0")
14 01010011 53(ascii"S")
15 01000001 41(ascii"A")
16 00000000 00
↓
30 00000000 00
31 0mmmmmmm mmmmmm - Memory number
32 0ddddd dddddd - data
↓
0sssssss ssssss - check_sum
11110111 F7
```

##### Dump request

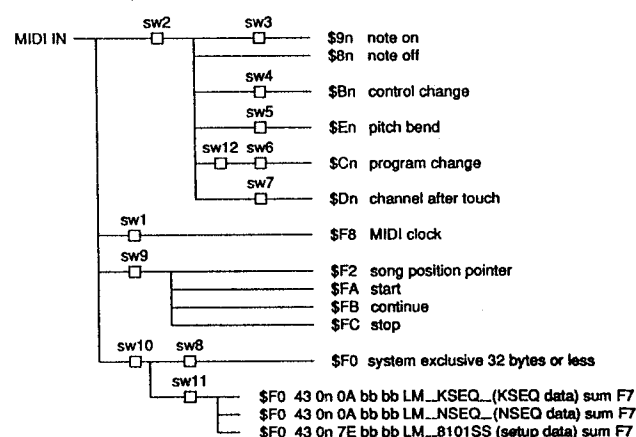
```
0 11110000 F0
1 01000011 43
2 0010nnnn nnnn - Device Number
3 01111010 7A
4 01001100 4C(ascii"L")
5 01001101 4D(ascii"M")
6 00100000 20(ascii" ")
7 00100000 20(ascii" ")
8 00110000 30(ascii"0")
9 00110000 30(ascii"0")
10 00110100 34(ascii"4")
11 00110000 30(ascii"0")
12 01010011 53(ascii"S")
13 01000001 41(ascii"A")
14 00000000 00
↓
28 00000000 00
29 0mmmmmmm mmmmmm - Memory number
30 11110111 F7
```

\* Refer to attached Table 9-2 for details regarding bulk dump data format.

#### 5. Sequencer mode

##### 5.1 MIDI reception/transmission block diagram

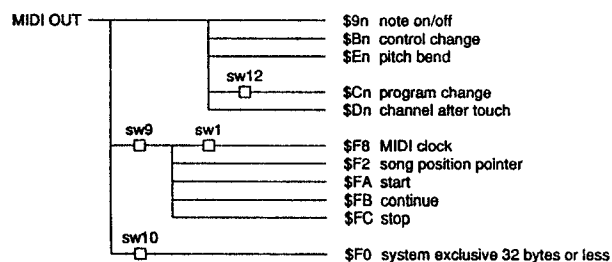
(Receive flow chart)



(Note)

- sw1 ☐ on when SEQ SETUP sync is set to MIDI
- sw2 ☐ during RECORD, the SEQ SETUP reception channel
- sw3 ☐ during RECORD, the SEQ SETUP velocity on/off
- sw4 ☐ during RECORD, the SEQ SETUP control change on/off
- sw5 ☐ during RECORD, the SEQ SETUP pitch bend on/off
- sw6 ☐ during RECORD, the SEQ SETUP program change on/off
- sw7 ☐ during RECORD, the SEQ SETUP channel pressure on/off
- sw8 ☐ during RECORD, the SEQ SETUP system exclusive (of 32 bytes or less) on/off
- sw9 ☐ on/off in SEQ SETUP for song position pointer, start, continue, stop
- sw10 ☐ set by the utility Device Number
- sw11 ☐ received only when utility Bulk Memory Protect = off
- sw12 ☐ received only when utility Program Change Mode is not off

(Transmit flow chart)



(Note)

- sw1 ☐ on when SEQ SETUP sync is set to INTERNAL  
 sw9 ☐ on/off in SEQ SETUP for MIDI clock song position pointer, start, continue, stop  
 sw10 ☐ set by the utility Device Number  
 sw12 ☐ received only when utility Program Change Mode is not off

## 5.2 Channel messages

Received only during RECORD. Transmitted only during PLAY and overdubbing.

For transmission and reception conditions, refer to the Receive flow chart and Transmit flow chart.

## 5.3 Mode messages

Neither received nor transmitted.

## 5.4 System common messages

Receive only \$F2 and \$F7. All others are neither received nor transmitted.

## 5.5 System realtime messages

### 5.5.1 Status F8, FA, FB, FC

Receive.

### 5.5.2 Status F9, FD, FF

After decoding, do nothing.

## 6. Status FE (active sensing)

### a) Transmission

Transmit FE at intervals of approximately 170 msec.

### b) Reception

Once FE has been received, if no MIDI data arrives for an interval longer than approximately 300 msec, the MIDI receive buffer is cleared, and if any keys remain on, they will be turned off.

&lt; Table 1-1 &gt;

MIDI Parameter Change table (Multi mode Common Data)

\$F0, \$43, \$1n, \$34, \$00, \$00, \$00, N2, \$00, V2, \$F7

Note) n ; Device Number

V2 ; parameter value

[header section]

	N2	data name	data range	note
0	00	MNAM 0	ascii	Multi Voice Set Name
1	01	MNAM 1	ascii	
2	02	MNAM 2	ascii	
3	03	MNAM 3	ascii	
4	04	MNAM 4	ascii	
5	05	MNAM 5	ascii	
6	06	MNAM 6	ascii	
7	07	MNAM 7	ascii	
8	08	MNAM 8	ascii	
9	09	MNAM 9	ascii	
10	0A	MNAM10	ascii	
11	0B	MNAM11	ascii	
12	0C	MNAM12	ascii	
13	0D	MNAM13	ascii	
14	0E	MNAM14	ascii	
15	0F	MNAM15	ascii	
16	10	MNAM16	ascii	
17	11	MNAM17	ascii	
18	12	MNAM18	ascii	
19	13	MNAM19	ascii	

&lt; Table 1-2 &gt;

MIDI Parameter Change table (Multi mode Channel Data)

\$F0, \$43, \$1n, \$34, \$01, T2, \$00, N2, \$00, V2, \$F7

Note) n ; Device Number

T2 ; voice channel number

V2 ; parameter value

[channel data]

	N2	data name	data range	note
0	00	OFVCSW INDV OUT0CH OUT1CH	b6 ; off/on b5~2 ; off, 1~8 b0 ; off/on b1 ; off/on	Channel 1 Off_voice_switch Individual Output select Output 1 select Output 2 select Note: INDV0 #3104 only valid. Voice Memory Select Voice number Volume Tuning Note shift Performance static PAN Note: Voice PAN setting not valid if a setting other than "voice" is selected.
1	01	VMEM	int, p1, p2, crd	
2	02	VNUM	0~63	
3	03	VOL	0~127	
4	04	MTUN	-64~+63 (o/b)	
5	05	MNSF	-64~+63 (o/b)	
6	06	STPAN	voice, -31~+31 (o/b)	
7	07	EFSDMD	voice/multi	effect send mode
8	08	EFLN1CH EFLN2CH EFLN3CH EFLN4CH	b0 ; off/on b1 ; off/on b2 ; off/on b3 ; off/on	effect send line 1 select effect send line 2 select effect send line 3 select effect send line 4 select
9	09	EFSDLV	0~127	effect send level

Note) (o/b) ; offset binary

&lt; Table 1-3 &gt;

MIDI Parameter Change table (Voice data common data)

\$F0, \$43, \$1n, \$34, \$02, \$00, \$00, N2, \$00, V2, \$f7

Note) n ; channel number  
V2 ; parameter value

[header data]

	N2	data name	data range	note
0	00	ELMODE	0: 1AFM_mono 1: 2AFM_mono 2: 4AFM_mono 3: 1AFM_poly 4: 2AFM_poly 5: 1AWM_poly 6: 2AWM_poly 7: 4AWM_poly 8: 1AFM_1AWM_poly 9: 2FM_2PCM_poly 10: DRUM_SET	—Element Select Mode—
1	01	VNAM0	ascii	—Voice Name— *
2	02	VNAM1	ascii	
3	03	VNAM2	ascii	
4	04	VNAM3	ascii	
5	05	VNAM4	ascii	
6	06	VNAM5	ascii	
7	07	VNAM6	ascii	
8	08	VNAM7	ascii	
9	09	VNAM8	ascii	
10	0A	VNAM9	ascii	

[Controllers]

	N2	data name	data range	note
11	28	WPBR	0~12	—Pitch Bend— Wheel Pitch Bend Range
12	29	ATPBR	-12~+12 (s/m)	After_Touch Pitch Bend Range
13	2A	PMASN	0~121	—Pitch Modulation— Device Assign (MIDI control #)
14	2B	PMRNG	0~127	Modulation range
15	2C	AMASN	0~121	—Amplitude Modulation— Device Assign (MIDI control #)
16	2D	AMRNG	0~127	Modulation range
17	2E	FMASN	0~121	—Filter Modulation— Device Assign (MIDI control #)
18	2F	FMRNG	0~127	Modulation range
19	30	PNLASN	0~121	—PAN Modulation— Note) Valid only when Multi is selected Device Assign (MIDI control #)
20	31	PNLRNG	0~127	Modulation range
21	32	COASN	0~121	—Filter Cut_off Bias— Device Assign (MIDI control #)
22	33	CORNG	0~127	Cut_off range
23	34	PNBASN	0~121	—PAN Bias— Note) Valid only when Multi is selected Device Assign (MIDI control #)
24	35	PNBRNG	0~127	Bias range
25	36	EGBASN	0~121	—EG Bias— Device Assign (MIDI control #)
26	37	EGBRNG	0~127	Bias range
27	38	VVLASN	0~121	—Voice Volume— Device Assign (MIDI control #)
28	39	VVLLML	0~127	Volume Limit Low

Note) For the above Device Assigns, 121 will select After Touch.

[Only for Normal]

	N2	data name	data range	note
29	3A	MCTUN	0~65	Micro Tuning table select
30	3B	RNDP	0~7	Random Pitch fluctuation
31	3C	PORM	0, 1	—Portamento— Note: Only valid in FM_Element only Voice modes.
32	3D	POS	0~127	Mode Time
33	3E	reserve		
34	3F	VVOL	0~127	Voice Volume
35	40	reserve		
36	41	reserve		
37	42	AFTMD	all, top, btm, hi, low	zoned after touch mode
38	43	SPTPNT	0~127	zoned after touch split point

Note) (s/m) ; sign magnitude

&lt; Table 1-4 &gt;

MIDI Parameter Change table (Normal Voice Element Data)

\$F0, \$43, \$1n, \$34, \$03, T2, \$00, N2, \$00, V2, \$F7

Note) n ; Device Number  
V2 ; parameter value  
T2 ; 0, e1, e0, 0, 0, 0, 0

e1	e0	
0	0	Element 1
0	1	Element 2
1	0	Element 3
1	1	Element 4

	N2	data name	data range	note
0	00	ELVL	0~127	Element Level
1	01	ELDT	-7~+7 (s/m)	Element Detune
2	02	ELNS	-64~+63 (o/b)	Element Note Shift
3	03	ENLL	0~127 (note #)	—Element Note Limit— Low Limit
4	04	ENLH	0~127 (note #)	High Limit
5	05	EVL	0~127 (note #)	—Element Velocity Limit— Low Limit
6	06	EVH	0~127 (note #)	High Limit
7	07	PANNM	0~31	PAN data set table select Note: Only valid when selected for Multi
8	08	MCTEN	b0: off/on	Micro Tuning switch
		OUTOSEL	b1: off/on	Output 1 select
		OUTISEL	b2: off/on	Output 2 select
9	09	EFLN1EL	b0: off/on	effect send line 1 select
		EFLN2EL	b1: off/on	effect send line 2 select
		EFLN3EL	b2: off/on	effect send line 3 select
		EFLN4EL	b3: off/on	effect send line 4 select
10	0A	EFSDLV	0~127	effect send level
11	0B	EFSDVL	-7~+7 (s/m)	effect send velocity sense
12	0C	EFSDSC	-7~+7 (s/m)	effect send level scale

Note) (s/m) ; sign magnitude  
(o/b) ; offset binary

&lt; Table 1-5 &gt;

MIDI Parameter Change table (Drum\_Set)

\$F0, \$43, \$1n, \$34, \$04, T2, \$00, N2, V1, V2, \$F7

Note) n ; channel number  
T2 ; MIDI note number  
N2 ; parameter number  
V1 ; MSB of parameter value (for parameters other than WAV\*,  
V1 will be \$00)  
V2 ; LSB of parameter value

	N2	data name	data range	note
0	00	ALTGRP	b6: 0~1	Alternate group
		OUT1	b1: 0~1	Output 2 select
		OUT0	b0: 0~1	Output 1 select
1	01	WSRC	0:Pre1 1:Card 2;—3:Int	Wave Source
2	02	WAV	4:Pre2 0~max. 255	Wave Number (V1:MSB V2:LSB7bits)
3	03	WVL	0~127	Wave Volume
4	04	WTN	-64~+63 (o/b)	Wave Tuning
5	05	WNS	-48~+36 (o/b)	Wave Note Shift
6	06	WPN	-31~+31 (o/b)	Static PAN
7	07	EFLN1C_1	b0: off/on	effect send line 1 select
		EFLN2C_1	b1: off/on	effect send line 2 select
		EFLN3C_1	b2: off/on	effect send line 3 select
		EFLN4C_1	b3: off/on	effect send line 4 select
8	08	EFSDVLC_1	0~127	effect send level
9	09	EFSDVLC_1	-7~+7 (s/m)	effect send velocity sense

Note) (o/b) ; offset binary

&lt; Table 1-6 &gt;

MIDI Parameter Change table (AFM Element Common)

\$F0, \$43, \$1n, \$34, \$05, T2, \$00, N2, \$00, V2, \$F7

Note) n ; Device Number  
 N2 ; parameter number  
 V2 ; parameter value

T2	
\$00	Element 1
\$20	Element 2
\$40	Element 3
\$60	Element 4

	N2	data name	data range	note
0	00	ALGNUM	0-44	(127 is free algorithm number. Algorithm only via MIDI)
1	01	FPR1	0-63	—Pitch EG— key_on Rate 1
2	02	FPR2	0-63	key_on Rate 2
3	03	FPR3	0-63	key_on Rate 3
4	04	FPRR1	0-63	key_off Rate 1
5	05	FPL0	-64~+63 (o/b)	key_on Level 0
6	06	FPL1	-64~+63 (o/b)	key_on Level 1
7	07	FPL2	-64~+63 (o/b)	key_on Level 2
8	08	FPL3	-64~+63 (o/b)	key_on Level 3
9	09	FPLR1	-64~+63 (o/b)	key_off Level 1
10	0A	FPEGR	0-3	Range (0: 8oct, 1: 2oct, 2: 1oct, 3: 1/2oct)
11	0B	FPRS	0-7	Rate Scaling
12	0C	FVPSW	off/on	Velocity Switch
13	0D	FLFSPD	0-99	—Main LFO— Speed
14	0E	FLFDLY	0-99	Delay time
15	0F	FLFMD	0-127	Pitch Modulation Depth
16	10	FLFAMD	0-127	Amplitude Modulation Depth
17	11	FLFFMD	0-127	Filter Modulation Depth
18	12	FLFWAV	0-5	Wave
19	13	FLINTP	0-99	Initial Phase
20	14	reserve		
21	15	SLFWD	0-3	—Sub LFO— Wave
22	16	SLFS	0-127	Speed
23	17	SLFDM	delay/decay	delay mode/decay mode
24	18	SLFDT	0-99	Delay time/decay time
25	19	SLPMD	0-127.	Pitch Modulation Depth

&lt; Table 1-7 &gt;

MIDI Parameter Change table (AFM Element)

\$F0, \$43, \$1n, \$34, T1, T2, \$00, N2, V1, V2, \$F7

Note) n ; Device Number  
 N2 ; parameter number  
 V1 ; MSB of parameter value  
 V2 ; LSB of parameter value

T1		T2	
\$06	OP6	\$00	Element 1
\$16	OP5	\$20	Element 2
\$26	OP4	\$40	Element 3
\$36	OP3	\$60	Element 4
\$46	OP2		
\$56	OP1		

	N2	data name	data range	note
0	00	R1	0-63	EG key_on Rate 1
1	01	R2	0-63	EG key_on Rate 2
2	02	R3	0-63	EG key_on Rate 3
3	03	R4	0-63	EG key_on Rate 4
4	04	RR1	0-63	EG key_off Rate 1
5	05	RR2	0-63	EG key_off Rate 2
6	06	L1	0-63	EG key_on Level 1
7	07	L2	0-63	EG key_on Level 2
8	08	L3	0-63	EG key_on Level 3
9	09	L4	0-63	EG key_on Level 4
10	0A	RL1	0-63	EG key_off Level 1
11	0B	RL2	0-63	EG key_off Level 2
12	0C	SLP	0-3	EG Sustain Loop Point
13	0D	HT	0-63 (disp: 63-0)	EG key_on/Hold Time
14	0E	LO	0-63	EG key_on Level 0
15	0F	RS	-7~+7 (s/m)	EG Rate Scaling
16	10	FAMS	0-7	Amplitude Modulation Sens.
17	11	VSON	-7~+7 (s/m)	Velocity Sensitivity
18	12	reserve		
19	13	ALGSR0	V2 b3-0 : 0-10	oscillator input 0 Source
20	14	ALGSR1	V1 b0, V2 b6-4 : 0-10	oscillator input 1 Source
		ALGDST	V2 b1, 0 : 0-3	oscillator output Destination
		OASCR0	V2 b3, 2 : 0-2	Out_Accumulator input 0 Source
		OASCR1	V2 b4 : 0-1	Out_Accumulator input 1 Source
21	15	SHIFT0	V2 b5-3 : 0-7	oscillator input 0 Shift value
		SHIFT1	V2 b2-0 : 0-7	oscillator input 1 Shift value
22	16	OCR	0-7	output level Correction
23	17	PWAVE	0-15	Waveform of oscillator
24	18	FMLPMS	V2 b4-2 : 0-7	M_LFO Pitch Modulation Sens.
		PES	V2 b1 : 0-1	Pitch EG Switch
		FFM	V2 b0 : 0-1	frequency Mode
25	19	KOE	V1 b0 : 0-1	initial phase set Enable
		PHASE	V2 b6-0 : 0-127	initial Phase of oscillator
26	1A	FPD	-15~+15 (s/m)	Pitch Detune

	N2	data name	data range	note
27	1B	TL	0-127	out_level
28	1C	BP1	0-127 (note #)	out_level scaling Break Point
29	1D	BP2	0-127 (note #)	out_level scaling Break Point
30	1E	BP3	0-127 (note #)	out_level scaling Break Point
31	1F	BP4	0-127 (note #)	out_level scaling Break Point
32	20	EGOS1	-128~+127 (2bytes)	out_level offset (BP1)
33	21	EGOS2	-128~+127 (2bytes)	out_level offset (BP2)
34	22	EGOS3	-128~+127 (2bytes)	out_level offset (BP3)
35	23	EGOS4	-128~+127 (2bytes)	out_level offset (BP4)
36	24	RVS	off/on	Rate Velocity Switch
37	25	FPC		frequency Course
38	26	FPF		frequency Fine

&lt; Table 1-8 &gt;

MIDI Parameter Change table (AFM Element)

\$F0, \$43, \$1n, #34, \$07, T2, \$00, N2, V1, V2, \$F7

Note) n ; Device Number  
 N2 ; parameter number  
 V1 ; MSB of parameter value  
 V2 ; LSB of parameter value  
 T2 ; table at right

T2	
\$00	Element 1
\$20	Element 2
\$40	Element 3
\$60	Element 4

[AWM generator unit]

	N2	data name	data range	note
0	00	WSOURCE	0: Pre1, 1: Card, 2: AFM, 3: Int, 4: Pre2	AWM Wave Source
1	01	AWMWAVE	V1: MSB1bit V2: LS7bits	AWM Wave number
2	02	PPM	normal/fixed	frequency Mode
3	03	PNOTE	0-127	fixed mode note #
4	04	PPF	-64~+63	frequency Fine
5	05	PMLPMS	0-7	pitch modulation sensitivity
6	06	PPR1	0-63	—Pitch EG— key_on Rate 1
7	07	PPR2	0-63	key_on Rate 2
8	08	PPR3	0-63	key_on Rate 3
9	09	PPRR1	0-63	key_off Rate 1
10	0A	PPL0	-64~+63 (o/b)	key_on Level 0
11	0B	PPL1	-64~+63 (o/b)	key_on Level 1
12	0C	PPL2	-64~+63 (o/b)	key_on Level 2
13	0D	PPL3	-64~+63 (o/b)	key_on Level 3
14	0E	PPRL1	-64~+63 (o/b)	key_off Level 1
15	0F	PPEGR	1-3	Range (1: 2oct, 2: 1oct, 3: 1/2oct)
16	10	PPRS	-7~+7	Rate Scaling
17	11	PVPSW	off/on	Velocity Switch
18	12	PLFSPD	0-99	—multi LFO— Speed
19	13	PLFDLY	0-99	Delay time
20	14	PLFMD	0-127	Pitch Modulation Depth
21	15	PLFAMD	0-127	Amplitude Modulation Depth
22	16	PLFFMD	0-127	Filter Modulation Depth
23	17	PLFWAV	0-5	Wave
24	18	PLINTP	0-99	Initial Phase
25	19	reserve		

[Amplitude EG data]

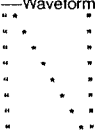
	N2	data name	data range	note
25	4F	PAEGMD	normal/hold	EG mode
26	50	PAR1	0-63	key_on Rate 1 (attack/hold)
27	51	PAR2	0-63	key_on Rate 2 (decay)
28	52	PAR3	0-63	key_on Rate 3
29	53	PAR4	0-63	key_on Rate 4 (decay)
30	54	PARR1	0-63	key_off Rate 1 (release)
31	55	PAL2	0-63	key_on Level 2 (decay)
32	56	PAL3	0-63	key_on Level 3 (decay)
33	57	PARS	-7~+7	rate scaling
34	58	PABP1	0-127 (note #)	out_level scaling Break Point
35	59	PABP2	0-127 (note #)	out_level scaling Break Point
36	5A	PABP3	0-127 (note #)	out_level scaling Break Point
37	5B	PABP4	0-127 (note #)	out_level scaling Break Point
38	5C	PAOS21	-128~+127 (2bytes)	out_level scaling offset
39	5D	PAOS22	-128~+127 (2bytes)	out_level scaling offset
40	5E	PAOS23	-128~+127 (2bytes)	out_level scaling offset
41	5F	PAOS24	-128~+127 (2bytes)	out_level scaling offset
42	60	PAVSON	-7~+7 (s/m)	Velocity Sensitivity
43	61	PARVSW	off/on	Attack Rate Velocity Switch
44	62	PAMS	-7~+7 (s/m)	amplitude modulation sens.

&lt; Table 1-9 &gt;

MIDI Parameter Change table (Waveform)

\$F0, \$43, \$1n, \$34, \$0E, \$T2, 05, N2, 00, V2, \$F7

Note) n ; Device Number  
 T2 ; Waveform number  
 N2 ; parameter number  
 V2 ; parameter value

	N2	data name	data range	note
0	00	WVNAME0	ascii	—Waveform Name— 
1	01	WVNAME1	ascii	
2	02	WVNAME2	ascii	
3	03	WVNAME3	ascii	
4	04	WVNAME4	ascii	
5	05	WVNAME5	ascii	
6	06	WVNAME6	ascii	
7	07	WVNAME7	ascii	
8	08	WVFROM	—, 1~99	Sample From
9	09	WVTO	—, 1~99	

&lt; Table 1-10 &gt;

MIDI Parameter Change table (Effect Data)

\$F0, \$43, \$1n, \$34, \$08, \$00, \$00, N2, \$00, V2, \$F7

Note) n ; Device Number  
 V2 ; parameter value

	N2	data name	data range	note
32	20	EFMODE	0~2	—Effect— mode select (off, seri, palla)
33	21	EF1TYPE	0~60	effect 1 type
34	22	EF1PRM1		effect 1 parameter 1
35	23	EF1PRM2		effect 1 parameter 2
36	24	EF1PRM3		effect 1 parameter 3
37	25	EF1PRM4		effect 1 parameter 4
38	26	EF1PRM5		effect 1 parameter 5
39	27	EF1PRM6		effect 1 parameter 6
40	28	EF1PRM7		effect 1 parameter 7
41	29	EF1PRM8		effect 1 parameter 8
42	2A	EF1PRM9		effect 1 parameter 9
43	2B	EF1PRM10		effect 1 parameter 10
44	2C	EF1OUTLV1	0~100	effect 1 output level 1
45	2D	EF1OUTLV2	0~100	effect 1 output level 2
46	2E	EF2TYPE	0~60	effect 2 type
47	2F	EF2PRM1		effect 2 parameter 1
48	30	EF2PRM2		effect 2 parameter 2
49	31	EF2PRM3		effect 2 parameter 3
50	32	EF2PRM4		effect 2 parameter 4
51	33	EF2PRM5		effect 2 parameter 5
52	34	EF2PRM6		effect 2 parameter 6
53	35	EF2PRM7		effect 2 parameter 7
54	36	EF2PRM8		effect 2 parameter 8
55	37	EF2PRM9		effect 2 parameter 9
56	38	EF2PRM10		effect 2 parameter 10
57	39	EF2FBAL1	0~100	effect 2 mix level
58	3A	EF2OUTLV1	0~100	effect 2 output level 1
59	3B	EF2OUTLV2	0~100	effect 2 output level 2
60	3C	OUT1EFBAL	0~100	output 1 effect balance wet/dry
61	3D	OUT2EFBAL	0~100	output 2 effect balance wet/dry
62	3E	CTRL1PRM	0~32	controller 1 parameter select
63	3F	CTRL1ASN	0~120, AT, VL, SC, LFO	controller 1 device assign
64	40	CTRL1MIN	0~99	controller 1 MIN
65	41	CTRL1MAX	0~99	controller 1 MAX
66	42	CTRL2PRM	0~32	controller 2 parameter select
67	43	CTRL2ASN	0~120, AT, VL, SC, LFO	controller 2 device assign
68	44	CTRL2MIN	0~99	controller 2 MIN
69	45	CTRL2MAX	0~99	controller 2 MAX
70	46	EFLFOV	tri, down, up, squ, sin, S/H	effect LFO wave select
71	47	EFLFOSF	0~99	effect LFO speed
72	48	EFLFODL	0~99	effect LFO delay time
73	49	EFLFOPH	0~99, free	effect LFO initial phase

&lt; Table 1-11 &gt;

MIDI Parameter Change table (Filter Data)

\$F0, \$43, \$1n, \$34, \$09, T2, \$00, N2, V1, V2, \$F7

Note) n ; Device Number  
 N2 ; parameter number  
 V1 ; MSB of parameter value  
 V2 ; LSB of parameter value  
 T2 ; O, E, E, O, O, N, N, N  
 (E, N table at right)

E	
00	Element 1
01	Element 2
10	Element 3
11	Element 4

N	
000	AFM filt. 1
001	AFM filt. 2
010	AMF common
011	AWM filt. 1
100	AWM filt. 2
101	AWM common

[filter 1 &amp; 2]

	N2	data name	data range	note
0	00	FTYPE	thru/LPF/(HPF)	filter type
1	01	FCTOF	0~127	cut_off frequency
2	02	FMODE	EG, LFO, EG-VA	filter mode
3	03	FR1	0~63	key_on Rate 1
4	04	FR2	0~63	key_on Rate 2
5	05	FR3	0~63	key_on Rate 3
6	06	FR4	0~63	key_on Rate 4
7	07	FRR1	0~63	key_off Rate 1
8	08	FRR2	0~63	key_off Rate 2
9	09	FL0	-64~+63 (o/b)	key_on cut_off Level 0
10	0A	FL1	-64~+63 (o/b)	key_on cut_off Level 1
11	0B	FL2	-64~+63 (o/b)	key_on cut_off Level 2
12	0C	FL3	-64~+63 (o/b)	key_on cut_off Level 3
13	0D	FL4	-64~+63 (o/b)	key_off cut_off Level 4
14	0E	FRL1	-64~+63 (o/b)	key_on cut_off Level 1
15	0F	FRL2	-64~+63 (o/b)	key_on cut_off Level 2
16	10	FRS	-7~+7	rate scaling
17	11	FBP1	0~127 (note #)	c_off_lv1 scaling Break Point
18	12	FBP2	0~127 (note #)	c_off_lv1 scaling Break Point
19	13	FBP3	0~127 (note #)	c_off_lv1 scaling Break Point
20	14	FBP4	0~127 (note #)	c_off_lv1 scaling Break Point
21	15	FOS1	-128~+127 (2bytes)	c_off_lv1 scaling offset
22	16	FOS2	-128~+127 (2bytes)	c_off_lv1 scaling offset
23	17	FOS3	-128~+127 (2bytes)	c_off_lv1 scaling offset
24	18	FOS4	-128~+127 (2bytes)	c_off_lv1 scaling offset

[filter common]


	N2	data name	data range	note
25	32	FRES	0~99	resonance
26	33	FVSON	-7~+7 (s/m)	Velocity Sensitivity
27	34	FCMS	-7~+7 (s/m)	Cut_off modulation sensitivity

&lt; Table 1-12 &gt;

MIDI Parameter Change table (Pan Data)

\$F0, \$43, \$1n, \$34, \$0A, T2, \$00, N2, \$00, V2, \$F7

Note) n ; Device Number  
 T2 ; Memory number  
 N2 ; parameter number  
 V2 ; parameter value

	N2	data name	data range	note
0	00	PNSCSEL	velocity, note #, LFO	PAN source select
1	01	PNSCDPT	0~99	PAN source depth
2	02	PNDT	0~63	—EG— key_on/Hold Time
3	03	PNR1	0~63	key_on Rate 1
4	04	PNR2	0~63	key_on Rate 2
5	05	PNR3	0~63	key_on Rate 3
6	06	PNR4	0~63	key_on Rate 4
7	07	PNRR1	0~63	key_off Rate 1
8	08	PNRR2	0~63	key_off Rate 2
9	09	PNL0	-32~+31 (o/b)	key_on Level 0
10	0A	PNL1	-32~+31 (o/b)	key_on Level 1
11	0B	PNL2	-32~+31 (o/b)	key_on Level 2
12	0C	PNL3	-32~+31 (o/b)	key_on Level 3
13	0D	PNL4	-32~+31 (o/b)	key_on Level 4
14	0E	PNRL1	-32~+31 (o/b)	key_off Level 1
15	0F	PNRL2	-32~+31 (o/b)	key_off Level 2
16	10	PNSLP	0~3	repeat segment
17	11	PNNAM0	ascii	—Dynamic PAN Name— 
18	12	PNNAM1	ascii	
19	13	PNNAM2	ascii	
20	14	PNNAM3	ascii	
21	15	PNNAM4	ascii	
22	16	PNNAM5	ascii	
23	17	PNNAM6	ascii	
24	18	PNNAM7	ascii	
25	19	PNNAM8	ascii	
26	1A	PNNAM9	ascii	

Note) (o/b) ; offset binary (invert the sign\_bit of the 2's complement)



&lt; Table 1-13 &gt;

MIDI Parameter Change table (Micro Tuning Data)

\$F0, \$43, \$1n, \$34, \$0B, T2, N1, N2, V1, V2, \$F7

Note) n ; Device Number

V1 ; MS7bits of parameter value

T2 ; memory number

V2 ; LS7bits of parameter value

	N1	N2	data name	data range	note
0	00	00	MCTC_2	0~10794	C_2
1	00	02	MCTC#2	0~10794	C#2
2	00	04	MCTD_2	0~10794	D_2
3	00	06	MCTD#2	0~10794	D#2
4	00	08	MCTE_2	0~10794	E_2
5	00	0A	MCTE#2	0~10794	E#2
6	00	0C	MCTF_2	0~10794	F_2
7	00	0E	MCTF#2	0~10794	F#2
8	00	10	MCTG_2	0~10794	G_2
9	00	12	MCTG#2	0~10794	G#2
10	00	14	MCTA_2	0~10794	A_2
11	00	16	MCTA#2	0~10794	A#2
12	00	18	MCTB_2	0~10794	B_2
13	00	1A	MCTB#2	0~10794	B#2
14	00	1C	MCTC_1	0~10794	C_1
15	00	1E	MCTC#1	0~10794	C#1
16	00	20	MCTD_1	0~10794	D_1
17	00	22	MCTD#1	0~10794	D#1
18	00	24	MCTE_1	0~10794	E_1
19	00	26	MCTE#1	0~10794	E#1
20	00	28	MCTF_1	0~10794	F_1
21	00	2A	MCTF#1	0~10794	F#1
22	00	2C	MCTG_1	0~10794	G_1
23	00	2E	MCTG#1	0~10794	G#1
24	00	30	MCTA_1	0~10794	A_1
25	00	32	MCTA#1	0~10794	A#1
26	00	34	MCTB_1	0~10794	B_1
27	00	36	MCTB#1	0~10794	B#1
28	00	38	MCTC_0	0~10794	C_0
29	00	3A	MCTC#0	0~10794	C#0
30	00	3C	MCTD_0	0~10794	D_0
31	00	3E	MCTD#0	0~10794	D#0
32	00	40	MCTE_0	0~10794	E_0
33	00	42	MCTE#0	0~10794	E#0
34	00	44	MCTF_0	0~10794	F_0
35	00	46	MCTF#0	0~10794	F#0
36	00	48	MCTG_0	0~10794	G_0
37	00	4A	MCTG#0	0~10794	G#0
38	00	4C	MCTA_0	0~10794	A_0
39	00	4E	MCTA#0	0~10794	A#0
40	00	50	MCTB_0	0~10794	B_0
41	00	52	MCTB#0	0~10794	B#0
42	00	54	MCTC_1	0~10794	C_1
43	00	56	MCTC#1	0~10794	C#1
44	00	58	MCTD_1	0~10794	D_1
45	00	5A	MCTD#1	0~10794	D#1
46	00	5C	MCTE_1	0~10794	E_1
47	00	5E	MCTE#1	0~10794	E#1
48	00	60	MCTF_1	0~10794	F_1
49	00	62	MCTF#1	0~10794	F#1
50	00	64	MCTG_1	0~10794	G_1
51	00	66	MCTG#1	0~10794	G#1
52	00	68	MCTA_1	0~10794	A_1
53	00	6A	MCTA#1	0~10794	A#1
54	00	6C	MCTB_1	0~10794	B_1
55	00	6E	MCTB#1	0~10794	B#1
56	00	70	MCTC_2	0~10794	C_2
57	00	72	MCTC#2	0~10794	C#2
58	00	74	MCTD_2	0~10794	D_2
59	00	76	MCTD#2	0~10794	D#2
60	00	78	MCTE_2	0~10794	E_2
61	00	7A	MCTE#2	0~10794	E#2
62	00	7C	MCTF_2	0~10794	F_2
63	00	7E	MCTF#2	0~10794	F#2
64	01	00	MCTG_2	0~10794	G_2
65	01	02	MCTG#2	0~10794	G#2
66	01	04	MCTA_2	0~10794	A_2
67	01	06	MCTA#2	0~10794	A#2
68	01	08	MCTB_2	0~10794	B_2
69	01	0A	MCTB#2	0~10794	B#2
70	01	0C	MCTC_2	0~10794	C_2
71	01	0E	MCTC#2	0~10794	C#2
72	01	10	MCTD_2	0~10794	D_2
73	01	12	MCTD#2	0~10794	D#2
74	01	14	MCTE_2	0~10794	E_2
75	01	16	MCTE#2	0~10794	E#2
76	01	18	MCTF_2	0~10794	F_2
77	01	1A	MCTF#2	0~10794	F#2
78	01	1C	MCTG_2	0~10794	G_2
79	01	1E	MCTG#2	0~10794	G#2
80	01	20	MCTA_2	0~10794	A_2
81	01	22	MCTA#2	0~10794	A#2
82	01	24	MCTB_2	0~10794	B_2
83	01	26	MCTB#2	0~10794	B#2
84	01	28	MCTC_2	0~10794	C_2
85	01	2A	MCTC#2	0~10794	C#2
86	01	2C	MCTD_2	0~10794	D_2
87	01	2E	MCTD#2	0~10794	D#2
88	01	30	MCTE_2	0~10794	E_2
89	01	32	MCTE#2	0~10794	E#2
90	01	34	MCTF_2	0~10794	F_2
91	01	36	MCTF#2	0~10794	F#2
92	01	38	MCTG_2	0~10794	G_2
93	01	3A	MCTG#2	0~10794	G#2
94	01	3C	MCTA_2	0~10794	A_2
95	01	3E	MCTA#2	0~10794	A#2
96	01	40	MCTB_2	0~10794	B_2

	N1	N2	data name	data range	note
97	01	42	MCTC#6	0~10794	C#6
98	01	44	MCTD_6	0~10794	D_6
99	01	46	MCTD#6	0~10794	D#6
100	01	48	MCTE_6	0~10794	E_6
101	01	4A	MCTE#6	0~10794	E#6
102	01	4C	MCTF_6	0~10794	F_6
103	01	4E	MCTF#6	0~10794	F#6
104	01	50	MCTG_6	0~10794	G_6
105	01	52	MCTG#6	0~10794	G#6
106	01	54	MCTA_6	0~10794	A_6
107	01	56	MCTA#6	0~10794	A#6
108	01	58	MCTB_6	0~10794	B_6
109	01	5A	MCTB#6	0~10794	B#6
110	01	5C	MCTC_7	0~10794	C_7
111	01	5E	MCTC#7	0~10794	C#7
112	01	60	MCTD_7	0~10794	D_7
113	01	62	MCTD#7	0~10794	D#7
114	01	64	MCTE_7	0~10794	E_7
115	01	66	MCTE#7	0~10794	E#7
116	01	68	MCTF_7	0~10794	F_7
117	01	6A	MCTF#7	0~10794	F#7
118	01	6C	MCTG_7	0~10794	G_7
119	01	6E	MCTG#7	0~10794	G#7
120	01	70	MCTA_7	0~10794	A_7
121	01	72	MCTA#7	0~10794	A#7
122	01	74	MCTB_7	0~10794	B_7
123	01	76	MCTB#7	0~10794	B#7
124	01	78	MCTC_8	0~10794	C_8
125	01	7A	MCTC#8	0~10794	C#8
126	01	7C	MCTD_8	0~10794	D_8
127	01	7E	MCTD#8	0~10794	D#8
128	02	00	MTNAM0	ascii	Micro Tuning Name
129	02	01	MTNAM1	ascii	.
130	02	02	MTNAM2	ascii	.
131	02	03	MTNAM3	ascii	.
132	02	04	MTNAM4	ascii	.
133	02	05	MTNAM5	ascii	.
134	02	06	MTNAM6	ascii	.
135	02	07	MTNAM7	ascii	.
136	02	08	MTNAM8	ascii	.
137	02	09	MTNAM9	ascii	.

&lt; Table 1-14 &gt;

MIDI Parameter Change table (Switch Remote)

\$F0, \$43, \$1n, \$34, \$0D, \$00, \$00, N2, \$00, V2, \$F7

Note) n ; Device Number

N2 ; parameter number

V2 ; parameter value data range : off (\$00~\$3F), on (\$40~\$7F)

	N2	sw.#	note
0	00	PSW 1	VOICE
1	01	PSW 2	MULTI
2	02	PSW 3	SONG
3	03	PSW 4	PATTERN
4	04	PSW 5	UTILITY
5	05	PSW 6	EDIT
6	06	PSW 7	STORE
7	07	PSW 8	EFFECT
8	08	PSW 9	I <
9	09	PSW10	<<
10	0A	PSW11	LOCATE
11	0B	PSW12	>>
12	0C	PSW13	RECORD
13	0D	PSW14	STOP
14	0E	PSW15	RUN
15	0F	PSW16	SHIFT
16	10	PSW17	F1
17	11	PSW18	F2
18	12	PSW19	F3
19	13	PSW20	F4
20	14	PSW21	F5
21	15	PSW22	F6
22	16	PSW23	F7
23	17	PSW24	F8
24	18	PSW25	EXIT
25	19	PSW26	PAGE <
26	1A	PSW27	PAGE >
27	1B	PSW28	JUMP
28	1C	PSW29	-1
29	1D	PSW30	↑
30	1E	PSW31	+1
31	1F	PSW32	↑
32	20	PSW33	↓
33	21	PSW34	→
34	22	PSW35	0
35	23	PSW36	±

	N2	sw.#	note
36	24	PSW37	ENTER
37	25	PSW38	1
38	26	PSW39	2
39	27	PSW40	3
40	28	PSW41	4
41	29	PSW42	5
42	2A	PSW43	6
43	2B	PSW44	7
44	2C	PSW45	8
45	2D	PSW46	9
46	2E	PSW47	INTERNAL
47	2F	PSW48	CARD
48	30	PSW49	PRESET 1
49	31	PSW50	PRESET 2
50	32	PSW51	A
51	33	PSW52	B
52	34	PSW53	C
53	35	PSW54	D
54	36	PSW55	1
55	37	PSW56	2
56	38	PSW57	3
57	39	PSW58	4
58	3A	PSW59	5
59	3B	PSW60	6
60	3C	PSW61	7
61	3D	PSW62	8
62	3E	PSW63	9
63	3F	PSW64	10
64	40	PSW65	11
65	41	PSW66	12
66	42	PSW67	13
67	43	PSW68	14
68	44	PSW69	15
69	45	PSW70	16
70	46	PSW71	DIAL DEC
71	47	PSW72	DIAL INC

&lt; Table 1-15 &gt;

## MIDI Parameter Change table (Master control)

\$F0, \$43, \$1n, \$34, \$0E, T2, N1, N2, V1, V2, \$F7

Note) n ; channel number  
 T2 ; control number  
 N1 ; parameter type  
 N2 ; parameter number  
 V1 ; MS7bits of parameter value  
 V2 ; LS7bits of parameter value

[Filter section] T2=00

	N1	N2	data name	data range	note
0	00	00	FILPGMMS	0-b'11111111	Program Change Filter ch 16-9
1	00	01	FILPGMLS	0-b'11111111	0:off 1:on ch 8-1
2	00	02	FILCONMS	0-b'11111111	Control Change Filter ch 16-9
3	00	03	FILCONLS	0-b'11111111	0:off 1:onch 8-1
4	00	04	FILPBDMS	0-b'11111111	Pitch Bend Filter ch 16-9
5	00	05	FILPBDLS	0-b'11111111	0:off 1:onch 8-1
6	00	06	FILSUSMS	0-b'11111111	Sustain Pedal Filter ch 16-9
7	00	07	FILSUSLS	0-b'11111111	0:off 1:onch 8-1
8	00	08	FILATCHMS	0-b'11111111	After Touch Filter ch 16-9
9	00	09	FILATCHLS	0-b'11111111	0:off 1:onch 8-1
10	00	0A	FILVOLMS	0-b'11111111	Main Volume Filter ch 16-9
11	00	0B	FILVOLLS	0-b'11111111	0:off 1:onch 8-1

[controller element section]

T2=0, 0, n, n, 0, t, t, t

n	
00	MIDI-1
01	MIDI-2
10	MIDI-3
11	MIDI-4

t	
000	Control 1
001	Control 2
010	Control 3
011	Control 4
100	Control 5
101	Control 6
110	Control 7
111	Control 8

	N1	N2	data name	data range	note
0	02	00	CONENABL	0-B'00011111	Control Enable 0:off 1:on Bit 0 = midi off/on 1 = pc off/on 2 = Ms/Ls off/on 3 = volume off/on 4 = MDR off/on
1	02	01	MIDITCH	0-15	MIDI Transmit Channel
2	02	02	NLIML	0-127	Note Limit Low
3	02	03	NLIMH	0-127	Note Limit High
4	02	04	VLIML	1-127	Velocity Limit Low
5	02	05	VLIMH	1-127	Velocity Limit High
6	02	06	XPOSE	0-127	Transpose [center 64 (40h)]
7	02	07	VELCURV	0-3	Velocity Curve
8	02	08	AFTCURV	0-3	After Touch Curve
9	02	09	MAINVOL	0-127	MAIN Volume
10	02	0A	BANK	0-16383	Bank Select
11	02	0C	PCNUM	0-127	Program Change Number
12	02	0D	MDRNUM	0-98	MDR Number

[Control name section]

T2=0, 0, 0, 0, 0, t, t, t

t	
000	Control 1
001	Control 2
010	Control 3
011	Control 4
100	Control 5
101	Control 6
110	Control 7
111	Control 8

	N1	N2	data name	data range	note
0	03	00	CNAM0	ascii	—Control Name—
1	03	01	CNAM1	ascii	
2	03	02	CNAM2	ascii	
3	03	03	CNAM3	ascii	
4	03	04	CNAM4	ascii	
5	03	05	CNAM5	ascii	
6	03	06	CNAM6	ascii	
7	03	07	CNAM7	ascii	
8	03	08	CNAM8	ascii	
9	03	09	CNAM9	ascii	

[Control voice section]

T2=0, 0, 0, 0, 0, t, t, t

t	
000	Control 1
001	Control 2
010	Control 3
011	Control 4
100	Control 5
101	Control 6
110	Control 7
111	Control 8

	N1	N2	data name	data range	note
0	04	00	FTM	off/on	Program
		01	VM	voice/multi	Program Mode
		02	VMEM	I/C/P1/P2	Program Memory
		03	VNUM	0-63	Voice Number
		04	MMEM	I/C/P	Multi Memory
		05	MNUM	0-15	Multi Number

&lt; Table 1-16 &gt;

## MIDI Parameter Change table (System Setup)

\$F0, \$43, \$1n, \$34, \$0F, \$00, \$00, N2, \$00, V2, \$F7

Note) n ; channel number  
 N2 ; parameter number  
 V2 ; parameter value

Note) Exception ; Master\_Tuning (at transmit) \$F0 \$43, \$1N, \$04, DT,  
 \$F7 (DX1 Master Tuning is used)

	N2	data name	data range	note
0	00	GRTMSU 0	ascii	—Greeting Message—
1	01	GRTMSU 1	ascii	Upper *
2	02	GRTMSU 2	ascii	Upper *
3	03	GRTMSU 3	ascii	Upper *
4	04	GRTMSU 4	ascii	Upper *
5	05	GRTMSU 5	ascii	Upper *
6	06	GRTMSU 6	ascii	Upper *
7	07	GRTMSU 7	ascii	Upper *
8	08	GRTMSU 8	ascii	Upper *
9	09	GRTMSU 9	ascii	Upper *
10	0A	GRTMSU10	ascii	Upper *
11	0B	GRTMSU11	ascii	Upper *
12	0C	GRTMSU12	ascii	Upper *
13	0D	GRTMSU13	ascii	Upper *
14	0E	GRTMSU14	ascii	Upper *
15	0F	GRTMSU15	ascii	Upper *
16	10	GRTMSU16	ascii	Upper *
17	11	GRTMSU17	ascii	Upper *
18	12	GRTMSU18	ascii	Upper *
19	13	GRTMSU19	ascii	Upper *
20	14	GRTMSL 0	ascii	Lower *
21	15	GRTMSL 1	ascii	Lower *
22	16	GRTMSL 2	ascii	Lower *
23	17	GRTMSL 3	ascii	Lower *
24	18	GRTMSL 4	ascii	Lower *
25	19	GRTMSL 5	ascii	Lower *
26	1A	GRTMSL 6	ascii	Lower *
27	1B	GRTMSL 7	ascii	Lower *
28	1C	GRTMSL 8	ascii	Lower *
29	1D	GRTMSL 9	ascii	Lower *
30	1E	GRTMSL10	ascii	Lower *
31	1F	GRTMSL11	ascii	Lower *
32	20	GRTMSL12	ascii	Lower *
33	21	GRTMSL13	ascii	Lower *
34	22	GRTMSL14	ascii	Lower *
35	23	GRTMSL15	ascii	Lower *
36	24	GRTMSL16	ascii	Lower *
37	25	GRTMSL17	ascii	Lower *
38	26	GRTMSL18	ascii	Lower *
39	27	GRTMSL19	ascii	Lower *
40	28	MNSFT	-64-63 (o/b)	Master Note Shift
41	29	MTUNE	-64-63 (o/b)	Master Fine Tuning (receive only)
42	2A	FIXVEL	off, 1-127	—Velocity—
43	2B	VELCRV	0-7	Fixed velocity Velocity Curve select
44	2C	MW2MCN	0-120	—MIDI Control Number Assign—
45	2D	FSASN	0-120	Modulation Wheel 2 Foot Switch assign
46	2E	EDCONFWS	off/on	Edit Confirm switch
47	2F	TXCH	0-15	—MIDI—
48	30	VRCH	0-15, omni	keyboard transmit channel
49	31	LOCAL	off/on	Voice Receive channel
50	32	DVCNUM	off, 0-15, all	Local switch
51	33	NTSW	all/odd/even	Device number
52	34	BLKMPRT	off/on	Note_Even_Odd switch
53	35	PGCMOD	off/on	Bulk data Memory protect switch
54	36	reserve		Program Change mode
55	37	PATPRT	off/on	Bulk Data Pattern Protect Switch

	N2	data name	data range	note
56	38	CONTHOLD	off/on	Controller Hold
57	39	MEMALOC	0~127	memory allocate for MDR (x4Kbyte)
58	3A	reserve		
59	3B	reserve		
60	3C	reserve		
61	3D	reserve		
62	3E	reserve		
63	3F	reserve		
	40	EBYP	0~2	Effect Bypass Sw (param cng only) 0:off 1:on Normal 2:on OUT-1 Direct OUT-2 Effect


**Note)** (o/b) ; offset binary (invert the sign\_bit of the 2's complement)

**< Table 1-17 >**

### MIDI Parameter Change table (Sample)

\$F0, \$43, \$1n, \$34, \$0E, \$T2, 06, N2, V1, V2, \$F7

Note) n ; Device Number  
T2 ; Sample number  
N2 ; parameter number  
V1 ; MS7bits of parameter value  
V2 ; LS7bits of parameter value

	N2	data name	data range	note
0 1 2	00 02 04	HIKEY ORIKEY PITCH	1~127 (note #) 0~127 (note #) -5376~+5376 (2bytes, o/b)	High key Original key Pitch
3	08	LOOPMODE	b2; 0 forward 1 backward b1; 0 loop off 1 loop on b0; 0 normal 1 alternate	Loop type, Mode
4 5	12 1C	VOL LOWKEY	0~127 1~127 (note #)	Volume Low key
6 7 8 9 10 11 12 13	1E 1F 20 21 22 23 24 25	SANAM0 SANAM1 SANAM2 SANAM3 SANAM4 SANAM5 SANAM6 SANAM7	ascii ascii ascii ascii ascii ascii ascii ascii	—Sample Name— 

**< Table 2-1 >**

## Voice Bulk Dump

Note) Memory\_type internal ; \$00  
 preset 1 ; \$02  
 preset 2 ; \$03  
 Edit Buffer ; \$7F (Used only when transmitting  
 from SY99. Memory# is transmitted  
 as \$00, ignored when receiving.)

When receiving Bulk dump, if Memory\_type is other than \$7F, this is processed as Internal.

Note) Memory#      \$00~\$0F    ; Bank A, 1~16  
                         \$10~\$1F    ; Bank B, 1~16  
                         \$20~\$2F    ; Bank C, 1~16  
                         \$30~\$3F    ; Bank D, 1~16

**Note)** When receiving Bulk dump, bit 6 of Memory# is ignored.

(1) 1AFM

data		Element1 data		Element1 data	
0	\$F0		Refer to 00~26 of Table 1-7.		Refer to 00~19 of Table 1-6.
1	\$43	107	OP6_R1	377	ALNUM
2	\$0N				
3	\$7A	125	reserve		
4	] byte count	126	OP6_ALGSRG (MSB)		
5		127	OP6_ALGSRG (low 7bits)		
6		128	OP6_ALGDST	403	Refer to 00~18 of Table 1-11.
7		132	OP6_FMPMS	423	FL1_FTYPE
8	L	133	OP6_K0E	424	FL1_FBP4
9	M	134	OP6_PHASE	425	FL1_FOS1 (MSB)
10		135	OP6_FPD	426	FL1_FOS1 (low 7bits)
11	8	140	OP6_BP4	427	FL1_FOS2 (MSB)
12	1	141	OP6_EGOS1 (MSB)	428	FL1_FOS2 (low 7bits)
13	0	142	OP6_EGOS2 (MSB)	429	FL1_FOS3 (MSB)
14	1	143	OP6_EGOS2 (low 7bits)	430	FL1_FOS3 (low 7bits)
15	V	144	OP6_EGOS3 (MSB)	431	FL1_FOS4 (MSB)
16	C	145	OP6_EGOS3 (low 7bits)		
17		146	OP6_EGOS4 (MSB)		
18	\$00	147	OP6_EGOS4 (low 7bits)	432	Refer to 00~18 of Table 1-11.
19		148	OP6_EGOS4 (MSB)		
20		149	OP6_RVSW	459	FL2_FOS4 (MSB)
21		150	OP6_PPC	460	FL2_FOS4 (low 7bits)
22		151	OP6_PPF		
23	Memory_type				
24	Memory#				
25					
26					
27					
28					
29					
30					
31					
32	Refer to 00~0A of Table 1-3.				
33	\$00 or \$03 (ELMODE) VNAMO				
34					
35					
36					
37					
38					
39					
40					
41					
42					
43	Refer to Dummy of Table 1-10.	152	Refer to 00~26 of Table 1-7.	461	Refer to 32~34 of Table 1-11.
44	EFMODE		OP5_R1	462	FFRES
45				463	FFVSON
46				464	FFCMS
47				465	check_sum
48					\$F7
49					
50					
51					
52					
53					
54					
55					
56					
57					
58					
59					
60					
61					
62					
63					
64					
65					
66					
67					
68					
69					
70					
71					
72	Refer to 28~3F of Table 1-3.	197	Refer to 00~26 of Table 1-7.		
73	WPBR		OP4_R1		
74					
75					
76					
77					
78					
79					
80					
81					
82					
83					
84					

## (2) 2AFM

data		Element1 data	
0	\$F0	116	Same as (1) AFM 107~463
1	\$43	↓	
2	\$0N	↓	
3	\$7A	472	
4	] byte count		
5			
6			
7	L	Element2 data	
8	M	473	Same as (1) AFM 107~463
9	-	↓	
10	8	829	
11	1		
12	0		
13	1		
14	V		
15	C		
16	] \$00		
17			
18			
29			
30	Memory_type		
31	Memory#		
32	\$01 or \$04 (ELMODE)		
33	] Same as (1) AFM 33~97		
34			
35			
97			
98	Refer to 00~08 of Table 1-4. ELVLO		
106	↓ MCTENO		
107	Refer to 00~08 of Table 1-4. ELVL1		
115	↓ MCTEN1		

## (4) 1AWM

data		Element1 data	
0	\$F0	116	Refer to 00~19 of Table 1-8. WSOURCE PCMWAVE (MSB) PCMWAVE (low 7bits) PPM
1	\$43	↓	
2	\$0N	↓	
3	\$7A	107	
4	byte count	108	Same as (1) AFM 403~463
5		109	
6		110	
7		134	
8	L	↓	
9	M	194	
10	—		
11	8		
12	0		
13	1		
14	V		
15	C		
16	\$00	195	Refer to 4F~62 of Table 1-8. PAEGMD PABP4 PAOS21 (MSB) PAOS21 (low 7bits) PAOS22 (MSB) PAOS22 (low 7bits) PAOS23 (MSB) PAOS23 (low 7bits) PAOS24 (MSB) PAOS24 (low 7bits) PAVSON PARVSW PAMS
17		207	
18		208	
19		209	
20	Memory_type	210	
21		211	
22	Memory#	212	
23		213	
24		214	
25		215	
26		216	
27		217	
28		218	
29		219	check_sum
30		220	
31			\$F7
32	\$05 (ELMODE)		
33	Same as (1) AFM 33~97		
34			
35			
36			
37			
38			
39			
40			
41			
42			
43			
44			
45			
46			
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90			
91			
92			
93			
94			
95			
96			
97			
98	Refer to 00~08 of Table 1-4. ELVLO		
99			
100	MCTEN0		
101			
102			
103			
104			
105			
106			

## (3) 4AFM

Note) Memory# : \$30~\$3F

When receiving, cancel if Memory# is other than the above.

data		Element1 data	
0	\$F0	134	Same as (1) AFM 107~463
1	\$43	↓	
2	\$0N	↓	
3	\$7A	490	
4	] byte count	Element2 data	
5			
6			
7			
8	L	491	Same as (1) AFM 107~463
9	M	↓	
10	—	847	
11	8		
12	0	Element3 data	
13	1		
14	V	848	Same as (1) AFM 107~463
15	C	↓	
16		1204	
17			
18	\$00	Element4 data	
19	Memory_type Memory#	1205	Same as (1) AFM 107~463
20		↓	
21		1561	
22			
23		1562	check_sum \$F7
24		1563	
25			
26			
27			
28			
29			
30			
31			
32	\$02 (ELMODE)		
33	Same as (1) AFM 33~97		
34			
35			
36			
37			
38			
39			
40			
41			
42			
43			
44			
45			
46			
47			
48			
49			
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90			
91			
92			
93			
94			
95			
96			
97			
98	Refer to 00~08 of Table 1-4. ELVLO		
99			
100	MCTEN0		
101			
102			
103			
104			
105			
106			
107	Refer to 00~08 of Table 1-4. ELVL1		
108			
109	MCTEN1		
110			
111			
112			
113			
114			
115			
116	Refer to 00~08 of Table 1-4. ELVL2		
117			
118	MCTEN2		
119			
120			
121			
122			
123			
124			
125	Refer to 00~08 of Table 1-4. ELVL3		
126			
127	MCTEN3		
128			
129			
130			
131			
132			
133			

## (5) 2AWM

data		Element1 data	
0	\$F0	116	Same as (1) 1AWM 107~218
1	\$43	↓	
2	\$0N	↓	
3	\$7A	227	
4	byte count	Element2 data	
5		Same as (1) 1AWM 107~218	228
6			↓
7			339
8			340
9	341		
10	L	check_sum	
11	M	\$F7	
12	—		
13	8		
14	0		
15	1		
16	V		
17	C		
18	\$00		
19			
20			
21			
22			
23	Memory_type		
24	Memory#		
25			
26			
27			
28			
29			
30			
31			
32	\$06 (ELMODE)		
33	Same as (1) AFM 33~97		
34			
35			
36			
37			
38			
39			
40			
41			
42			
43			
44			
45			
46			
47			
48			
49			
50			
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89			
90			
91			
92			
93			
94			
95			
96			
97			
98	Refer to 00~08 of Table 1-4. ELVLO		
99			
100	↓		
101	MCTENO		
102			
103			
104			
105			
106			
107	Refer to 00~08 of Table 1-4. ELVL1		
108			
109	↓		
110	MCTEN1		
111			
112			
113			
114			
115			

## (6) 4AWM

	data		Element1 data		
0	\$F0	134	Same as (1) 1AWM 107~218		
1	\$43	↓			
2	\$0N	↓			
3	\$7A	245			
4	byte count	Element2 data			
5		Same as (1) 1AWM 107~218	Element2 data		
6			246		
7			↓		
8	357				
9	L	Element3 data			
10	M	Same as (1) 1AWM 107~218	Element3 data		
11	—		358		
12	8		↓		
13	1		469		
14	0	Same as (1) 1AWM 107~218	Element4 data		
15	V		Same as (1) 1AWM 107~218	Element4 data	
16	C			470	
↓	\$00			↓	
29		581			
30		582			
31		583			
32	\$07 (ELMODE)	check_sum			
33	Same as (1) AFM 33~97	\$F7			
↓					
↓					
97					
98	Refer to 00~08 of Table 1-4. ELVL0	MCTEN0			
106					
107	Refer to 00~08 of Table 1-4. ELVL1	MCTEN1			
115					
116	Refer to 00~08 of Table 1-4. ELVL2	MCTEN2			
124					
125	Refer to 00~08 of Table 1-4. ELVL3	MCTEN3			
133					

## (8) 2AFM\_2AWM

Note) Memory# ; \$30~\$3F

When receiving, cancel if Memory# is other than the above.

	data		Element1 data
0	\$F0	134	Same as (1) AFM 107-463
1	\$43	↓	
2	\$0N	↓	
3	\$7A	490	
4	byte count		
5			
6			
7			
8	L		Element2 data
9	M	491	Same as (1) AFM 107-463
10	—	↓	
11	8	847	
12	1		
13	0		
14	1		Element3 data
15	V		Same as (1) 1AWM 107-218
16	C	848	
↓	\$00	↓	
29		959	
30			
31			
32	Memory_type		Element4 data
33	Memory#		Same as (1) 1AWM 107-218
32	\$09 (ELMODE)	960	
33	Same as (1) AFM 33-97	↓	
↓		1071	
↓			
97			
98	Refer to 00-08 of Table 1-4. ELVL0	1072	check_sum \$F7
↓	↓	1073	
106	MCTEN0		
107	Refer to 00-08 of Table 1-4. ELVL1		
↓	↓		
115	MCTEN1		
116	Refer to 00-08 of Table 1-4. ELVL2		
↓	↓		
124	MCTEN2		
125	Refer to 00-08 of Table 1-4. ELVL3		
↓	↓		
133	MCTEN3		

## (7) 1AFM\_1AWM

data		Element1 data	
0	\$F0	116	Same as (1) AFM 107~463
1	\$43	↓	
2	\$0N	↓	
3	\$7A	472	
4	] byte count	Element2 data	
5		] Same as (4) 1AWM 107~218	
6			
7			
8			
9	L	473	
10	M	↓	
11	-	584	
12	8		
13	1	585	check_sum
14	0	586	
15	1		
16	V		
17	C	\$F7	
↓	] \$00		
29			
30		Memory_type	
31		Memory#	
32	\$08 (ELMODE)		
33	] Same as (1) AFM 33~97		
↓			
↓			
97			
98	Refer to 00~08 of Table 1-4. ELVL0	MCTEN0	
↓			
106			
107	Refer to 00~08 of Table 1-4. ELVL1	MCTEN1	
↓			
115			

## (9) Drum\_set

data		Drum_set data		Drum_set data	
0	\$F0	98	ALTC_1, OUT*C_1	194	ALTC_2, OUT*C_2
1	\$43	99	WSRCC_1	↓	↓
2	\$0N	100	WAVC_1 (MSB)	↓	↓
3	\$7A	101	WAVC_1 (low 7bits)	290	ALTC_3, OUT*C_3
4	byte count	102	WVLC_1	↓	↓
5		103	WTNC_1	↓	↓
6		104	WNSC_1	↓	↓
7		105	WPNC_1	386	ALTC_4, OUT*C_4
8	—	106	ALTC#1, OUT*C#1	↓	↓
9	↓	↓	↓	↓	↓
10	8	↓	↓	↓	↓
11	1	114	ALTD_1, OUT*D_1	482	ALTC_5, OUT*C_5
12	0	↓	↓	↓	↓
13	1	122	ALTD#1, OUT*D1	↓	↓
14	V	↓	↓	578	ALTC_6, OUT*C_6
15	C	130	ALTE_1, OUT*E_1	↓	↓
↓	\$00	↓	↓	585	WPNC_6
29		138	ALTF_1, OUT*F_1	↓	↓
30		↓	↓	586	check_sum
31		146	ALTF#1, OUT*F#1	587	\$F7
32	\$0A (ELMODE)	↓	↓		
33	↓	154	ALTG_1, OUT*G_1		
↓	↓	↓	↓		
71	↓	162	ALTG#1, OUT*G#1		
72	\$00 (ctrl)	↓	↓		
87		170	ALTA_1, OUT*A_1		
88		↓	↓		
89		178	ALTA#1, OUT*A#1		
↓	\$00 (norm)	↓	↓		
90		186	ALTB_1, OUT*B_1		
95		↓	↓		
96		↓	↓		
97	AWMID high 7	↓	↓		
	AWMID low 7	↓	↓		



## (10) dump request

	data
0	\$F0
1	\$43
2	\$2N
3	\$7A
4	L
5	M
6	-
7	-
8	8
9	1
10	0
11	1
12	V
13	C
14	↓
15	\$00
27	↓
28	Memory_type
29	Memory#
30	\$F7

\* Memory\_type = not \$7F (edit buffer)

## &lt; Table 2-2 &gt;

## Additional Voice Bulk Dump

Note) Memory\_type internal ; \$00  
 preset 1 ; \$02  
 preset 2 ; \$03  
 Edit Buffer ; \$7F (Used only when transmitting from SY99. Memory# is transmitted as \$00, ignored when receiving.)

For WSOURCE, AWMWAV, data which has the same name exists in the Voice Bulk Dump which is the AWM Element data shown in table 1-8, but when Voice Bulk and Additional Voice Bulk are transmitted together, Additional bulk WSOURCE, AWMWAV becomes effective.

When receiving Bulk dump, if Memory\_type is other than \$7F, this is processed as Internal.

Note) Memory# \$00-\$0F ; Bank A, 1~16  
 \$10-\$1F ; Bank B, 1~16  
 \$20-\$2F ; Bank C, 1~16  
 \$30-\$3F ; Bank D, 1~16

Note) When receiving Bulk dump, bit 6 of Memory# is ignored.

## (1) 1AFM &amp; 1AWM

	data
0	\$F0
1	\$43
2	\$0N
3	\$7A
4	↓
5	byte count
6	L
7	M
8	-
9	-
10	0
11	0
12	4
13	0
14	V
15	C
16	↓
17	\$00
29	↓
30	Memory_type
31	Memory#
32	Refer to 00 of Table 1-3. \$00, \$03, \$05 (ELMODE)
33	Refer to 20~5D of Table 1-10. EFMODE
95	AWMID high 7bit
96	AWMID low 7bit
97	AFTMD
98	SPTPNT
99	Refer to 09~12 of Table 1-4. EFLN1EL0
100	EFSDLV0
101	EFSDVL0
102	EFSDSC0
103	WSOURCE1
104	AWMWAV (MSB)
105	AWMWAV (low 7bit)
106	check_sum
107	\$F7

## (2) 2AFM &amp; 2AFM &amp; 1AFM\_1AWM

	data
0	\$F0
1	\$43
2	\$0N
3	\$7A
4	↓
5	byte count
6	L
7	M
8	-
9	-
10	0
11	0
12	4
13	0
14	V
15	C
16	↓
17	\$00
29	↓
30	Memory_type
31	Memory#
32	Refer to 00 of Table 1-3. \$01, \$04, \$06, \$08 (ELMODE)
33	Refer to 20~5D of Table 1-10. EFMODE
95	AWMID high 7bit
96	AWMID low 7bit
97	AFTMD
98	SPTPNT
99	Refer to 09~12 of Table 1-4. EFLN1EL0
100	EFSDLV0
101	EFSDVL0
102	EFSDSC0
103	Refer to 09~12 of Table 1-4. EFLN1EL1
104	EFSDLV1
105	EFSDVL1
106	EFSDSC1

107	WSOURCE1
108	AWMWAV (MSB)
109	AWMWAV (low 7bit)
110	WSOURCE2
111	AWMWAV (MSB)
112	AWMWAV (low 7bit)
113	check_sum
114	\$F7

## (3) 4AFM &amp; 4AWM &amp; 2AFM\_2AWM

Note) Memory# ; \$30-\$3F

When receiving, cancel if Memory# is other than the above.

	data
0	\$F0
1	\$43
2	\$0N
3	\$7A
4	↓
5	byte count
6	L
7	M
8	-
9	-
10	0
11	0
12	4
13	0
14	V
15	C
16	↓
17	\$00
29	↓
30	Memory_type
31	Memory#
32	Refer to 00 of Table 1-3. \$02, \$07, \$09 (ELMODE)
33	Refer to 20~5D of Table 1-10. EFMODE
95	AWMID high 7bit
96	AWMID low 7bit
97	AFTMD
98	SPTPNT
99	Refer to 09~12 of Table 1-4. EFLN1EL0
100	EFSDLV0
101	EFSDVL0
102	EFSDSC0
103	Refer to 09~12 of Table 1-4. EFLN1EL1
104	EFSDLV1
105	EFSDVL1
106	EFSDSC1

107	Refer to 09~12 of Table 1-4. EFLN1EL2
108	EFSDLV2
109	EFSDVL2
110	EFSDSC2
111	Refer to 09~12 of Table 1-4. EFLN1EL3
112	EFSDLV3
113	EFSDVL3
114	EFSDSC3
115	WSOURCE1
116	AWMWAV (MSB)
117	AWMWAV (low 7bit)
118	WSOURCE2
119	AWMWAV (MSB)
120	AWMWAV (low 7bit)
121	WSOURCE3
122	AWMWAV (MSB)
123	AWMWAV (low 7bit)
124	WSOURCE4
125	AWMWAV (MSB)
126	AWMWAV (low 7bit)
127	check_sum
128	\$F7

## (4) Drum\_set

data	
0	\$F0
1	\$43
2	\$0N
3	\$7A
4	byte count
5	L
6	M
7	-
8	-
9	0
10	0
11	4
12	0
13	V
14	C
15	
16	\$00
29	
30	Memory_type
31	Memory#
32	Refer to 00 of Table 1-3. \$0A (ELMODE)
33	Refer to 20~5D of Table 1-10. EFMODE
95	AWMID high 7bit
96	AWMID low 7bit
97	AFTMD
98	SPTPNT
99	Refer to 07~09 of Table 1-5.
100	WSOURCEC_1
101	AWMWAV (MSB)
102	AWMWAV (low 7bit)
103	EFLN1C_1
104	EFSDVLC_1
105	EFSDVLC_1
459	WSOURCEC_6
460	AWMWAV (MSB)
461	AWMWAV (low 7bit)
462	EFLN1C_6
463	EFSDVLC_6
464	EFSDVLC_6

465	Refer to 07~09 of Table 1-5. ALTE_0
531	ALTB_0
541	EFSDVLC_0
542	ALTC#_6
619	ALTG_6
629	ALTG_6
630	WSOURCEC_0
631	AWMWAV (MSB)
632	AWMWAV (low 7bit)
663	WSOURCEC_6
664	AWMWAV (MSB)
665	AWMWAV (low 7bit)
666	check_sum
667	\$F7

&lt; Table 3-1 &gt;

## Multi Bulk Dump

Note) Memory\_type internal ; \$00  
 preset ; \$02  
 Edit Buffer ; \$7F (Used only when transmitting  
 from SY99. Memory# is transmitted  
 as \$00, ignored when receiving.)

When receiving Bulk dump, if Memory\_type is other than \$7F, this is  
 processed as Internal.

Note) Memory# \$00~\$0F ; INT1~16

Note) When receiving Bulk dump, bits 6~4 of Memory# are ignored.

data		data		data	
0	\$F0	90	Refer to 00~06 of Table 1-2. OFVCSW_0, OUT*CH_0	0	\$F0
1	\$43	97	OFVCSW_1, OUT*CH_1	1	\$43
2	\$0N	104	OFVCSW_2, OUT*CH_2	2	\$2N
3	\$7A	111	OFVCSW_3, OUT*CH_3	3	\$7A
4	byte count	118	OFVCSW_4, OUT*CH_4	4	L
5	L	125	OFVCSW_5, OUT*CH_5	5	M
6	M	132	OFVCSW_6, OUT*CH_6	6	-
7	-	139	OFVCSW_7, OUT*CH_7	7	-
8	-	146	OFVCSW_8, OUT*CH_8	8	0
9	0	153	OFVCSW_9, OUT*CH_9	9	0
10	0	160	OFVCSW10, OUT*CH10	10	4
11	4	167	OFVCSW11, OUT*CH11	11	0
12	0	174	OFVCSW12, OUT*CH12	12	M
13	0	181	OFVCSW13, OUT*CH13	13	U
14	M	188	OFVCSW14, OUT*CH14	14	
15	U	195	OFVCSW15, OUT*CH15	27	\$00
16		201	STPAN15	28	Memory type
29	\$00	202	check_sum	29	Memory#
30	Memory_type	203	\$F7	30	\$F7
31	Memory#				
32	Refer to 00~13 of Table 1-1. MNAME0				
51	MNAME19				
52	Refer to Dummy of Table 1-10. EFMODE				
80	ST_MIX2				

\* Memory type =  
not \$7F  
(Edit buffer)

&lt; Table 3-2 &gt;

## Additional Multi Bulk Dump

Note) Memory\_type internal ; \$00  
 preset ; \$02  
 Edit Buffer ; \$7F (Used only when transmitting  
 from SY99. Memory# is transmitted  
 as \$00, ignored when receiving.)

When receiving Bulk dump, if Memory\_type is other than \$7F, this is  
 processed as Internal.

Note) Memory # \$00~\$0F ; INT1~16

Note) When receiving Bulk dump, bits 6~4 of Memory# are ignored.

## (5) dump request

data	
0	\$F0
1	\$43
2	\$2N
3	\$7A
4	L
5	M
6	-
7	-
8	0
9	0
10	4
11	0
12	V
13	C
14	
27	\$00
28	Memory type
29	Memory#
30	\$F7

\* Memory type = not \$7F (edit buffer)

data		data		data	
0	\$F0	95	Refer to 07~09 of Table 1-2. EFSDMD0	0	\$F0
1	\$43	98	EFSDMD1	1	\$43
2	\$0N	101	EFSDMD2	2	\$2N
3	\$7A	104	EFSDMD3	3	\$7A
4	byte count	107	EFSDMD4	4	L
5	L	110	EFSDMD5	5	M
6	M	113	EFSDMD6	6	-
7	-	116	EFSDMD7	7	-
8	-	119	EFSDMD8	8	0
9	0	122	EFSDMD9	9	0
10	0	125	EFSDMD10	10	4
11	4	128	EFSDMD11	11	0
12	0	131	EFSDMD12	12	M
13	0	134	EFSDMD13	13	U
14	M	137	EFSDMD14	14	
15	U	140	EFSDMD15	27	\$00
16		143	check_sum	28	Memory type
29	\$00	144	\$F7	29	Memory#
30	Memory_type			30	\$F7
31	Memory#				
32	Refer to 20~5D of Table 1-10. EFMODE				
94	EFLFOPH				

\* Memory type =  
not \$7F  
(Edit buffer)

&lt; Table 4 &gt;

## Pan Bulk Dump

Note) Memory\_type internal ; \$00  
 preset ; \$02

When receiving Bulk dump, processed as Internal regardless of the Memory\_type.

Note) Memory# \$00~\$1F ; INT1~32

Note) When receiving Bulk dump, bits 6, 5 of Memory# are ignored.

dump request		data	
0	\$F0	0	\$F0
1	\$43	1	\$43
2	\$0N	2	\$2N
3	\$7A	3	\$7A
4	byte count	4	L
5	L	5	M
6	M	6	-
7	-	7	-
8	-	8	8
9	-	9	1
10	8	10	0
11	1	11	1
12	0	12	P
13	1	13	N
14	P	14	↓
15	N	15	\$00
16	↓	27	↓
29	\$00	28	Memory type
30	Memory_type	29	Memory#
31	Memory#	30	\$F7
32	Refer to 00~1A of Table 1-12.		
33	PNCSSEL		
58	PNNAM9		
59	check_sum		
60	\$F7		

&lt; Table 5 &gt;

## Micro Tuning Bulk Dump

Note) Memory# \$00~\$01 ; INT1~2

Note) When receiving Bulk dump, bits 6~1 of Memory# are ignored.

dump request		data	
0	\$F0	0	\$F0
1	\$43	1	\$43
2	\$0N	2	\$2N
3	\$7A	3	\$7A
4	byte count	4	L
5	L	5	M
6	M	6	-
7	-	7	-
8	-	8	8
9	-	9	1
10	8	10	0
11	1	11	1
12	0	12	M
13	1	13	T
14	M	14	↓
15	T	15	\$00
16	↓	27	↓
29	\$00	28	\$00
30	\$00	29	Memory#
31	Memory#	30	\$F7
32	Refer to 0000~017E of Table 1-13.		
33	MCTC_2 (high 7bits)		
286	↓		
287	MCTG_8 (high 7bits)		
	↓		
	MCTG_8 (low 7bits)		
288	Refer to 0200~0209 of Table 1-13.		
289	MTNAM_1		
290	↓		
291	MTNAM10		
292	check_sum		
293	\$F7		

&lt; Table 6 &gt;

## Master Control Bulk Dump

dump request		data	
0	\$F0	58	CONENA1_1
1	\$43	71	MDRNUM1_1
2	\$0N	72	CONENA2_1
3	\$7A	85	MDRNUM2_1
4	byte count	86	CONENA3_1
5	L	99	MDRNUM3_1
6	M	100	CONENA4_1
7	-	113	MDRNUM4_1
8	-		
9	-	114	CONENA1_2
10	0	505	MDRNUM4_8
11	0		
12	4	506	CNAM0_1
13	0	515	CNAM9_1
14	M		
15	S	516	CNAM0_2
16	↓	585	CNAM9_8
31	\$00	586	PGM_1
32	Refer to Table 1-15.	591	MNUM_1
33	FILPGMH (MSB)		
34	FILPGMH (low 7 bits)	592	PGM_2
35	FILPGML (MSB)	633	MNUM_8
52	FILMVOLH (MSB)		
53	FILMVOLH (low 7 bits)	634	check_sum
54	FILMVOLL (MSB)	635	\$F7
55	FILMVOLL (low 7 bits)		
56	reserved		
57	reserved		

&lt; Table 7 &gt;

## System Setup Bulk Dump

dump request		data	
0	\$F0	0	\$F0
1	\$43	1	\$43
2	\$0N	2	\$2N
3	\$7A	3	\$7A
4	byte count	4	L
5	L	5	M
6	M	6	-
7	-	7	-
8	-	8	8
9	-	9	1
10	8	10	0
11	1	11	1
12	0	12	S
13	1	13	Y
14	S	14	↓
15	Y	15	\$00
16	↓	29	↓
31	\$00	30	\$F7
32	Refer to 00~3F of Table 1-16.		
95	↓		
	reserve		
96	check_sum		
97	\$F7		

&lt; Table 8-1 &gt;

## Sequencer Setup Bulk Dump

		dump request	
data		data	
0	\$F0	0	\$F0
1	\$43	1	\$43
2	\$0N	2	\$2N
3	\$7E	3	\$7E
4	byte count	4	L
5	L	5	M
6	M	6	-
7	-	7	-
8	-	8	-
9	-	9	-
10	0	10	0
11	1	11	1
12	0	12	S
13	1	13	S
14	S	14	\$F7
15	S		
16	QUANTIZE		
17	CLICK SWITCH		
18	CLICK BEAT		
19	reserve		
20	SYNC MODE		
21	REC MIDI CHANNEL		
22	VELOCITY SW.		
23	CONTROL CHANGE SW.		
24	PITCH BEND SW.		
25	PROGRAM CHANGE SW.		
26	AFTER TOUCH SW.		
27	SYSEXCLUSIVE SW.		
28	MIDI CONTROL SW.		
29	EDIT BEAT/CLOCK		
30	ACCENT1		
31	ACCENT2		
32	ACCENT3		
33	ACCENT4		
34	GATE TYPE		
35	check_sum		
36	\$F7		

&lt; Table 9-1 &gt;

## Waveform Data Bulk Dump

Note) FROM, TO When Memory\_type of \$01 (card), \$02 or \$03 (pre1), or \$04 (pre2) is specified, FROM and TO are both set to a value of \$00.

		data	
0	\$F0	0	\$F0
1	\$43	1	\$43
2	\$0N	2	\$0N
3	\$7A	3	\$7A
4	byte count	4	byte count
5	L	5	L
6	M	6	M
7	-	7	-
8	-	8	-
9	-	9	-
10	0	10	0
11	0	11	0
12	4	12	4
13	0	13	0
14	W	14	W
15	V	15	V
16	↓	16	↓
29	↓	29	↓
30	Memory_type	30	Memory_type
31	Memory#	31	Memory#
32	Refer to 0-9 of Table 1-9.	32	Refer to 0-9 of Table 1-9.
33	WVNAME0	33	WVNAME0
34	↓	34	↓
39	WVNAME7	39	WVNAME7
40	WVFROM	40	WVFROM
41	WVTO	41	WVTO
42	check_sum	42	check_sum
43	\$F7	43	\$F7

&lt; Table 8-2 &gt;

## Sequencer Song &amp; Pattern (KSEQ, NSEQ) Bulk Dump

KSEQ and NSEQ data is converted from 1 byte to 2 byte ascii data and transmitted. The data for one song consists of more than one track of data, where each track begins with F0 0n, (n=track number) and ends with F2. Empty tracks will not be included.

hex	description
F0	top of record track #1
00	
---	time/event/control data
F2	end of record track #1
---	track #2-#15 data
F0	top of record track #16
0F	
---	time/event/control data
F2	end of record track #16

&lt; Table 9-2 &gt;

## Sample data Bulk Dump

		data	
0	\$F0	0	\$F0
1	\$43	1	\$43
2	\$0N	2	\$0N
3	\$7A	3	\$7A
4	byte count	4	byte count
5	L	5	L
6	M	6	M
7	-	7	-
8	-	8	-
9	-	9	-
10	0	10	0
11	0	11	0
12	4	12	4
13	0	13	0
14	S	14	S
15	A	15	A
16	↓	16	↓
30	↓	30	↓
31	Memory#	31	Memory#
32	Refer to 6-13 of Table 1-17.	32	Refer to 6-13 of Table 1-17.
33	SANAM0	33	SANAM0
34	↓	34	↓
39	SANAM7	39	SANAM7
40	HIKEYCODEH (MSB)	40	HIKEYCODEH (MSB)
41	HIKEYCODEH (low 7bit)	41	HIKEYCODEH (low 7bit)
42	HIKEYCODEL (MSB)	42	HIKEYCODEL (MSB)
43	HIKEYCODEL (low 7bit)	43	HIKEYCODEL (low 7bit)
44	ORKEY	44	ORKEY
45	PITCHCODEH (MSB)	45	PITCHCODEH (MSB)
46	PITCHCODEH (low 7bit)	46	PITCHCODEH (low 7bit)
47	PITCHCODEL (MSB)	47	PITCHCODEL (MSB)
48	PITCHCODEL (low 7bit)	48	PITCHCODEL (low 7bit)
49	LOOPMODE	49	LOOPMODE
50	VOLCODE (MSB)	50	VOLCODE (MSB)
51	VOLCODE (low 7bit)	51	VOLCODE (low 7bit)
52	LOWKEYCODEH (MSB)	52	LOWKEYCODEH (MSB)
53	LOWKEYCODEH (low 7bit)	53	LOWKEYCODEH (low 7bit)
54	LOWKEYCODEL (MSB)	54	LOWKEYCODEL (MSB)
55	LOWKEYCODEL (low 7bit)	55	LOWKEYCODEL (low 7bit)
56	check_sum	56	check_sum
57	\$F7	57	\$F7

Function ...	Transmitted	Recognized	Remarks
Basic Default	1 - 16	1 - 16	memorized
Channel Changed	1 - 16	1 - 16	
Mode Default	x	x	
Messages	x	x	
Altered	*****	x	
Note Number : True voice	0 - 127 *****	0 - 127	
Velocity Note ON	o 9nH,v=1-127	o v=1-127	
Note OFF	x 9nH,v=0	x	
After Key's	x	x	
Touch Ch's	o	o	
Pitch Bender	o	o	
0 - 120	o	o	
Control Change			
Prog Change : True #	o 0 - 127 *****	o 0 - 127	
System Exclusive	o	o	Song data etc.
: Song Pos	o	o	
Common : Song Sel	o	o	
: Tune	x	x	
System :Clock	o	o	
Real Time :Commands	o	o	
Aux :Local ON/OFF	x	x	
:All Notes OFF	x	x	
Mes- :Active Sense	x	x	
sages:Reset	x	x	
Notes			

Mode 1 : OMNI ON, POLY  
Mode 3 : OMNI OFF, POLY

Mode 2 : OMNI ON, MONO  
Mode 4 : OMNI OFF, MONO

o : Yes  
x : No



Function ...		Transmitted	Recognized	Remarks	
Basic	Default	1 - 16	1 - 16	memorized	
Channel	Changed	1 - 16	1 - 16		
Mode	Default	3	1,2,3,4	memorized	
	Messages	x	x		
	Altered	*****	x		
Note		28 - 103	0 - 127		
Number :	True voice	*****	1 - 127		
Velocity	Note ON	o 9nH,v=1-127	o v=1-127		
	Note OFF	x 9nH,v=0	x		
After	Key's	x	x		
Touch	Ch's	o	o		
Pitch Bender		o	o 0-12 semi	7 bit resolution	
Control	0	o	o	Bank select	
	1	o M.Wheel	o		
	2	o Breath cont.	o		
	4	o Foot cont.	o		
	Change	6	o Data entry	o	Volume Bank select Sustain Portamento
		7	o Foot volume	o	
		32	o	o	
		64	o Sustain sw.	o	
		65	o Portamento sw	o	
		96	o inc.	o	
97	o dec.	o			
1 - 6	o Assignable	o			
8 - 120	o Assignable	o			
Prog		o 0-79 *1	o 0-79		
Change :	True #	*****	*2		
System Exclusive		o	o	voice etc.	
: Song Pos					
Common : Song Sel					
: Tune		See the sequencer part.			
System :Clock					
Real Time :Commands					
Aux	:Local ON/OFF	x	x		
	:All Notes OFF	x	x		
Mes-	:Active Sense	o	o		
sages:	Reset	x	x		
Note *1 ; Send PC,Master control: 0 - 127					
*2 ; voice : 0 - 63 , multi : 64 - 79					

Mode 1 : OMNI ON, POLY    Mode 2 : OMNI ON, MONO    o : Yes  
Mode 3 : OMNI OFF, POLY    Mode 4 : OMNI OFF, MONO    x : No

# MUSIC SYNTHESIZER

# SY99

# PARTS LIST

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## Note) DESTINATION ABBREVIATIONS

J : Japanese model	A : Australian model
U : U.S. model	E : European model
C : Canadian model	D : German model
X : General model	B : British model
M : South African model	I : Indonesian model
H : North European model	

# ELECTRICAL PARTS (電気部品)

Ref. No.	Part No.	Description	部 品 名	Remarks	ランク
	VK287400	Circuit Board	DM1	SY99	66
	VK287500	Circuit Board	DM2		90
	VK261900	Circuit Board	P N A B		19
	VK261800	Circuit Board	P N C		23
	VJ875400	Circuit Board	J K		
	NX809690	Circuit Board	J K (J K)		
	NX809700	Circuit Board	J K (J K B)		
	NX809710	Circuit Board	J K (C A R D)		
	VK666500	Circuit Board	C N		
	NA810850	Circuit Board	M K 1		07
	NA810860	Circuit Board	M K 2		08
	VK263600	Circuit Board	P C		08
	VJ800200	Circuit Board	P S	J	19
	VJ800300	Circuit Board	P S	U	20
	VJ800400	Circuit Board	P S	C	20
	VJ800500	Circuit Board	P S	H, D, A, B	20
	VK287400	Circuit Board	DM1		66
	IG001390	IC	RC4558D-V	OP AMP	03
	XH970A00	IC	M62021L	RESET	04
	IG043300	IC	TC4093BP	NAND	05
	IG049650	IC	SN74LS14N	INVERTER	05
	IR001450	IC	SN74HC14N	INVERTER	05
	XA055001	IC	SN74ALS32N	OR	03
	IG149600	IC	SN74ALS138N	DECODER	04
	IG149900	IC	SN74ALS245AN	BUS TRANSCEIVER	07
	IR024500	IC	TC74HC245AP	BUS BUFFER	07
	XH608A00	IC	TC74AC245P	BUS TRANSCEIVER	05
	IR405200	IC	TC74HC4052AP	MULTIPLEXER	03
	XI722000	IC	H8/532	CPU	
	XF148A00	IC	HD63C01Y0F64P	CPU	09
	XG950C00	IC	HD63B01Y0RM21P	PKS	08
	XB361001	IC	$\mu$ PD71055C	PPI	06
	XH129B00	IC	WD37C65C-JM00	FDD CONTROLLER	15
	XI500A00	IC	LZ95B12	GATE ARRAY	05
	XI501A00	IC	LZ95A13	GATE ARRAY	05
	XE612A00	IC	HM658128P-12	PSRAM	17
	XF876A00	IC	LH5164D-10L	SRAM	08
	XH266A00	IC	HM62256LP-10	SRAM	13
	XI580A00	IC	HM628128LP-10	SRAM	22
	XJ613D00	IC	TC574000D	EPROM (040AV120)	
	XJ614B00	IC	HN27C101AG	EPROM (040BV110)	
	XJ615C00	IC	HN27C101AG	EPROM (040CV120)	
	XJ616C00	IC	M5M27C201K	EPROM (040DV120)	
	VD473200	Photo Coupler	6N137	フォト カ プ ラ	05
	IC260320	Transistor	2SC2603 E, F	ト ラ ン ジ ス タ	01
	IF003450	Diode	1SS133	ダ イ オード	01
	VB481900	Diode	11ES4	ダ イ オード	01
	VA074400	Metal Film Resistor	10K $\Omega$ 1/5W F	金 属 皮 膜 抵 抗	01
	HZ004650	Resistor Array	RMLS6J103	抵 抗 ア レ イ	02
	VA823000	Resistor Array	RMLS6-223J	抵 抗 ア レ イ	01
	VE443500	Resistor Array	RGLD4X103J	抵 抗 ア レ イ	01
	VE445200	Resistor Array	RGLD8X103J	抵 抗 ア レ イ	01
	VE445400	Resistor Array	RGLD8X223J	抵 抗 ア レ イ	01
	VG284400	Resistor Array	RMLS7J103	抵 抗 ア レ イ	01
	VK409500	Resistor Array	RMLS5J102	抵 抗 ア レ イ	01
	VK437400	Resistor Array	RMLS7153J	抵 抗 ア レ イ	01
	RD254470	Chip Resistor	47 $\Omega$ 0.1W J	チ ャ ッ プ 抵 抗	01
	RD255100	Chip Resistor	100 $\Omega$ 0.1W J	チ ャ ッ プ 抵 抗	01
	RD256100	Chip Resistor	1K $\Omega$ 0.1W J	チ ャ ッ プ 抵 抗	01
	RD256470	Chip Resistor	4.7K $\Omega$ 0.1W J	チ ャ ッ プ 抵 抗	01
	RD257100	Chip Resistor	10K $\Omega$ 0.1W J	チ ャ ッ プ 抵 抗	01
	UJ838470	Electrolytic Cap.	470 $\mu$ 16V	チ ケ ミ コ ン	01
	VJ798800	Chip Monolithic Cera. Cap.	F 0.1 $\mu$ 25V Z	チ ャ ッ プ 積 層 セ ラ コ ン	01
	FZ006970	EMI Filter	LS MT Y223NB	L C フ ィ ル ター E M I	02
	VE463500	Quartz Crystal Unit	12MHz AT-49	水 晶 振 動 子	03
	VI573400	Quartz Crystal Unit	16MHz AT-49	水 晶 振 動 子	03
	VK409400	Quartz Crystal Unit	24MHz AT-49	水 晶 振 動 子	03
	VE338400	Lithium Battery	SONY/CR2032	リ ュ ム 電 池	03
	VH930600	Metal Fitting, Earth		アース 金 具	01
	VK287500	Circuit Board	DM2		90
	IG042500	IC	NJM4556		04
	XJ748A00	IC	M5238P R610	OP AMP.	03
	IG065510	IC	NJM78L05A	+5V REGULATOR	03
	IG130500	IC	NJM79L05	-5V REGULATOR	03
	XH970A00	IC	M62021L	RESET	04
	XD655A00	IC	TC74HC00AF-TP1	NAND	01
	XJ622A00	IC	TC74HC21AF	2-4 IN AND	01

\*New Parts (新規部品)

ランク : Japan only

Ref. No.	Part No.	Description	部 品 名	Remarks	ランク
	XC726001	IC	SN74HC74NSR	DFF	03
	XD835A00	IC	SN74HC138NSR	DECODER	02
	XD658A00	IC	TC74HC175AF-TP1	DFF	02
	XD603A00	IC	TC74HC245F-T1	TRANSCEIVER	04
	XE057A00	IC	SN74ALS245ANSR	BUFFER	05
	XH779A00	IC	SN74LS245ANSR	BUFFER	03
	XJ623A00	IC	TC74HC4051AF	MULTIPLEXER	02
	XG662A00	IC	TMC57800N	MIX5	07
	XH690A00	IC	PCM56P-Y	DAC	07
	XI364A00	IC	LC9116A-483	TW80 DECODER	07
	XF237A00	IC	YM3029	DAC	09
	XE862B00	IC	YM3422B	ESI	05
	XA902001	IC	YM3807	MOD	09
	XF164A00	IC	YM6007	DSP2	18
	XG996A00	IC	YM7102	PAN	10
	XG993A00	IC	YM7103	EGW2	13
	XG994A00	IC	YM7107	OPS3	13
	XG995A00	IC	YM7119	M3	18
	XD265A00	IC	MB81464-12PSZ	DRAM 256K	08
	XI580A00	IC	HM628128LP-10	SRAM 1M	22
	XI728A00	IC	LH538087	ROM 8M	13
	XI729A00	IC	LH538088	ROM 8M	13
	XI730A00	IC	LH538089	ROM 8M	13
	XI731B00	IC	TC538200P-H099	ROM 8M	
	XI732A00	IC	MB838200-20P-G	ROM 8M	13
	XI733A00	IC	MB838200-20P-G	ROM 8M	13
	XI734A00	IC	MB838200-20P-G	ROM 8M	13
	XI735B00	IC	TC538200P-H100	ROM 8M	
	IA111510	Transistor	2SA1115 E,F	トランジスタ	01
	IC287820	Transistor	2SC2878 A,B	トランジスタ	01
	VD488500	Digital Transistor	DTC143XS TP	デジタルトランジスタ	03
	IF003450	Diode	1SS133	ダイオード	01
	VE443500	Resistor Array	RGLD4X103J	抵抗アレイ	01
	VE445200	Resistor Array	RGLD8X103J	抵抗アレイ	01
	RD255100	Chip Resistor	100Ω 0.1W J	チップ抵抗	01
	VB593200	Trimmer Potentiometer	B100K EVN	半固定抵抗	01
	VC694800	Semiconductive Cera. Cap.	0.1μ 25V Z	半導体セラコン	01
	VJ798800	Chip Monolithic Cera. Cap.	F 0.1μ 25V Z	チップ積層セラコン	01
	FZ006970	EMI Filter	LS MT Y223NB	LC フィルター EMI	02
	VI552000	Quartz Crystal Unit	AF2138CG	水晶振動子	03
	VE338400	Lithium Battery	SONY/CR2032	リチウム電池	03
	VH930600	Metal Fitting, Earth		アース金具	01
	VK261900	Circuit Board	PNAB	P N A B シート	19
	IA101521	Transistor	2SA1015 Y	トランジスタ	01
	IF003450	Diode	1SS133	ダイオード	01
	VG197400	LED	GL3HD18 RE	LED	01
	VG197600	LED	GL3ED8	2色LED	01
	VH812000	LED Spacer	× 8	LEDスパーサー	02
	VH812100	LED Spacer	× 4	LEDスパーサー	01
	VE373500	Slide Pot.	A10K × 2	二連スライダポリューム	03
	VF946200	Push Switch	SOA-111HS	プッシュスイッチ	01
	VK261800	Circuit Board	PNC	P N C シート	23
	IR027350	IC	SN74HC273N	IC	05
	IF003450	Diode	1SS133	ダイオード	01
	VG197400	LED	GL3HD18 RE	LED	01
	VG197600	LED	GL3ED8	2色LED	01
	VH812000	LED Spacer	× 8	LEDスパーサー	02
	VC250600	Slide Pot.	B10K EVA-NFOC	スライドポリューム	03
	VC694800	Semiconductive Cera. Cap.	0.1μ 25V Z	半導体セラコン	01
	VB436400	Rotary Switch	EC24B30D	ロータリースイッチ	07
	VF946200	Push Switch	SOA-111HS	プッシュスイッチ	01
	VJ875400	Circuit Board	JK	J K シート	
	NX809690	Circuit Board	JK (JK)	J K (J K) シート	
	NX809700	Circuit Board	JK (JKB)	J K (J K B) シート	
	NX809710	Circuit Board	JK (CARD)	J K (C A R D) シート	
	IC094530	Transistor	2SC945A PA	トランジスタ	01
	IF003450	Diode	1SS133	ダイオード	01
	VD048800	Variable Resistor	A10K EVU-E	ロータリーポリューム	02
	VI573700	Variable Resistor	B1K EVU-E2A	ロータリーポリューム	02
	VC694800	Semiconductive Cera. Cap.	0.1μ 25V Z	半導体セラコン	01
	VK458100	DC/AC Inverter Transformer	D32-49A	D C / A C インバータトランス	07
	VB835000	Coil	20μ H FL5R200QN	コイル	01
	LB203090	Phone Jack	STEREO HLJ0521	ホーンジャック	02
	LB301780	Phone Jack	STEREO HLJ4306	ホーンジャック	03
	LB302010	Phone Jack	ST.MINI HSJ0912	ホーンジャック	02
	VE742000	Phone Jack	MONO HLJ4306	ホーンジャック	02

\*New Parts (新規部品)

ランク: Japan only

Ref. No.	Part No.	Description	部 品 名	Remarks	ランク
	VE742200	Phone Jack	STEREO HLJ4306	F.VOLUME,F.CONT	02
	VI662400	Phone Jack	STEREO. HLJ4306	OUTPUT2 (L/R)	02
	LB500520	DIN Jack	5P TCS4650-01	MIDI(IN,OUT,THR	03
	VF821100	Connector, IC Card	IC3A-38PS-1.27D	38P DATA	06
	VH985300	Connector, IC Card	264D-550P-28D8	50P WAVEFORM	08
	VC362700	Ferrite Core	FR25/15/12-1400	2pcs	04
	CR069250	Cord Clamper	BK-1	3pcs	01
	AA833840	Angle Bracket, C.B.			01
	VH812200	Angle Bracket-H, Jack			03
	VH812300	Angle Bracket-M, Jack			02
	ED040066	Bind Head Screw	4.0×6 ZMC2Y	バインド小ネジ	01
	VK666500	Circuit Board	CN	C N シート	
	IR013800	IC	TC74HC138AP	DECODER-8	05
	VF169200	Resistor Array	RMLS5 J 473	抵抗 アレイ	01
	VC694800	Semiconductive Cera. Cap.	0.1μ 25V Z	半導体セラコン	01
	VD542700	EMI Filter	DSS306-93F223Z1	L C フィルター E M I	01
	LB903400	Connector HIF	40P SE	H I F コネクタ	07
	VI347400	Connector FX2	52P SE	F X 2 コネクタ	04
	NA810850	Circuit Board	MK1	M K 1 シート	07
	IF003450	Diode	1SS133	ダイオード	01
	NA810860	Circuit Board	MK2	M K 2 シート	08
	IF003450	Diode	1SS133	ダイオード	01
	LB920300	Connector	30P SE	コネクタ	06
	ED040066	Bind Head Screw	4.0×6 ZMC2Y	バインド小ネジ	01
	VK263600	Circuit Board	PC	P C シート	08
	IG001390	IC	RC4558D-V	I C	03
	VA240700	Diode	1SS176	ダイオード	01
	VI692000	Zener Diode	05A Z5.1V 5.1V	ツェナーダイオード	01
	HT370250	Trimmer Potentiometer	B5K 3P EVN	半固定抵抗	02
	HT370260	Trimmer Potentiometer	B100K 3P EVN	半固定抵抗	02
	VJ800200	Circuit Board	PS	P S シート	19
	VJ800300	Circuit Board	PS	P S シート	20
	VJ800400	Circuit Board	PS	P S シート	20
	VJ800500	Circuit Board	PS	P S シート	20
	IG136200	IC	SI-3052V	I C	06
	XD340001	IC	AN78M12F	I C	03
	XD342001	IC	AN79M12F	I C	03
	VB481900	Diode	11ES4	ダイオード	01
	IH001210	Diode Stack	S4VB20	ダイオードスタック	04
	IH001370	Diode Stack	D5FB20 5A 200V	ダイオードスタック	05
	VD488400	Diode Stack	DF04M 1A 400V	ダイオードスタック	02
	IF010780	Zener Diode	MTZ6.8C 6.8V	ツェナーダイオード	01
	VC745800	Metal Oxide Film Resistor	220Ω 1W J	酸化金属皮膜抵抗	01
	F1383220	Ceramic Cap.	2200P 400V	規格認定コン	01
	F1383470	Ceramic Cap.	4700P 400V	規格認定コン	01
	FI494100	Ceramic Cap.	0.01μ 400V	規格認定コン	01
	UJ63A100	Electrolytic Cap.	10000μ 16V	ケミコン	04
	UJ649100	Electrolytic Cap.	1000μ 25V	ケミコン	02
	UJ649220	Electrolytic Cap.	2200μ 25V	ケミコン	03
	VC694800	Semiconductive Cera. Cap.	0.1μ 25V Z	半導体セラコン	01
	GD900760	Coil	3mH PLA3021A	コイル	06
	VF576000	Push Switch	ESB-8236V JUCS	プッシュスイッチ	03
	KB000400	Fuse	T 5A 250V	ヒューズ	01
	KB000420	Fuse	T 2.5A 250V	ヒューズ	01
	KB002590	Fuse	T 5A 250V	ヒューズ	02
	KB002650	Fuse	T 3A 250V	ヒューズ	03
	KB002680	Fuse	T 2.5A 250V	ヒューズ	03
	KB000690	Fuse	T2.5A 250V S	ヒューズ	02
	KB000780	Fuse	T5A 250V S	ヒューズ	02
	LB201530	Fuse Holder	PC-FH1	ヒューズホルダー	01
	VA855400	Terminal		P C 用カラゲ端子	01
	IL000680	Insulation Sheet	BFG-20	放熱シート	01
	--	Heat Sink		放熱板	01
	VK355400	Angle Bracket, Pw. Switch		P S アングル	05
	E1030106	Bind Head Tapping Screw	3.0×10 ZMC2Y	バインドタッピングネジ	01
	E1040106	Bind Head Tapping Screw	4.0×10 ZMC2Y	バインドタッピングネジ	01
	VK372800	LCD Assembly		L C D A s s ' y	
	VF931200	LCD	DMF5005NYL-EW	液晶ディスプレイ	28
	VK588200	Variable Resistor	10K RK1241110	ロータリーボリューム	03
	HS412160	Variable Resistor	10K K161100S	ロータリーボリューム	03
	VI666700	Variable Resistor	10K RK1631110	ロータリーボリューム	03

\*New Parts (新規部品)

ランク: Japan only



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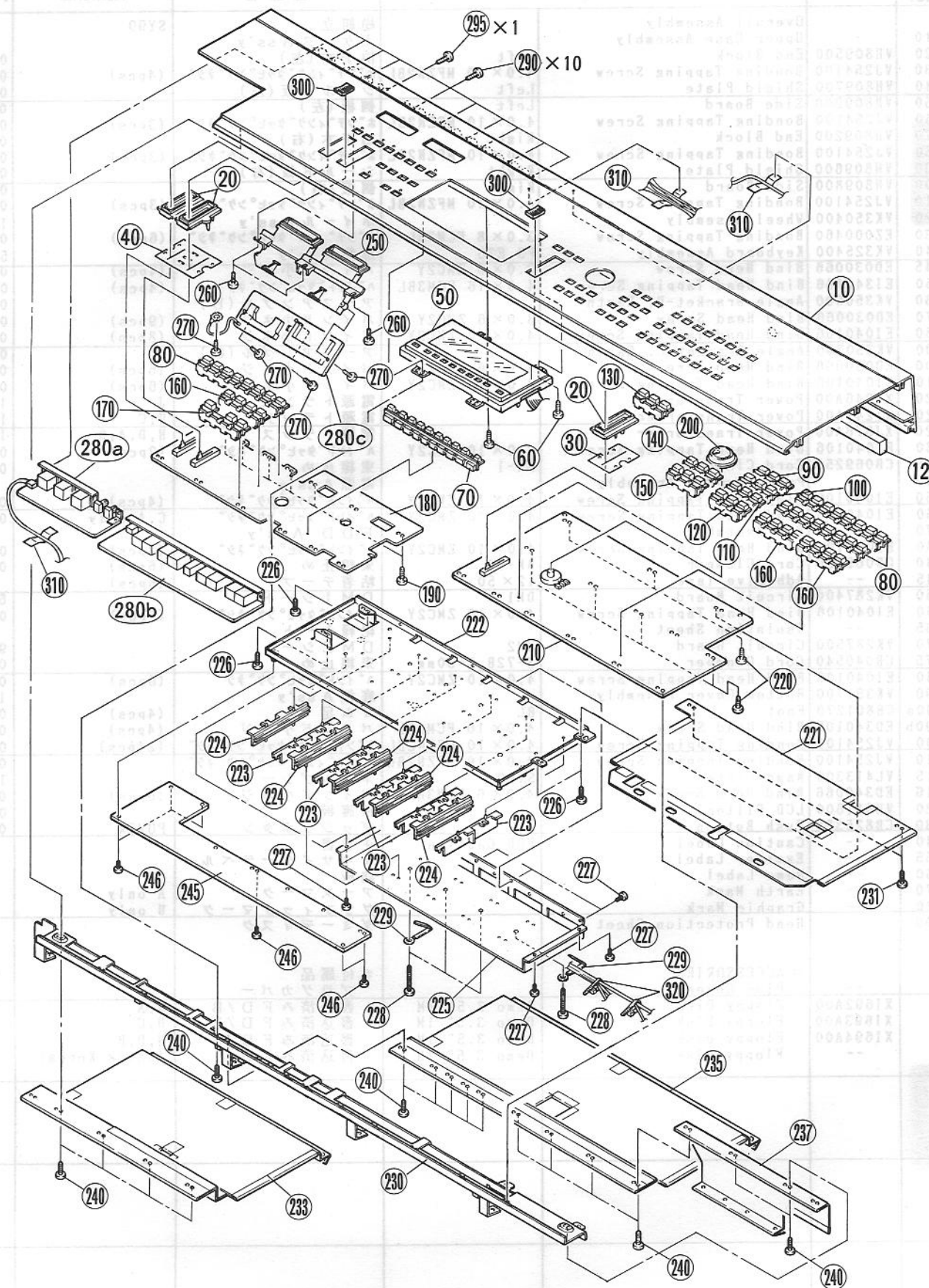


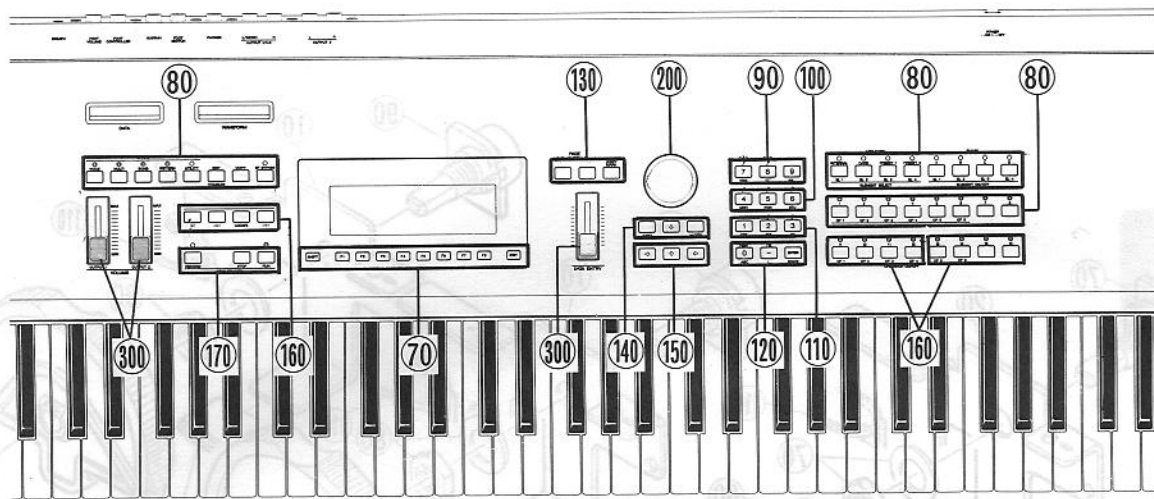
Ref. No.	Part No.	Description	部 品 名	Remarks	ランク
10	--	Overall Assembly	総組立	SY99	
20	VH809500	Upper Case Assembly	上ケース Ass'y		
30	VJ254100	End Block	拍子木 (左)		09
40	VH809700	Bonding Tapping Screw	ボンドインクタッピングネジ	(4pcs)	01
50	VH809900	Shield Plate	シールド板 (左)		07
60	VJ254100	Side Board	側板 (左)		04
70	VH809200	Bonding Tapping Screw	ボンドインクタッピングネジ	(3pcs)	01
80	VJ254100	End Block	拍子木 (右)		07
90	VH809600	Bonding Tapping Screw	ボンドインクタッピングネジ	(3pcs)	01
100	VH809800	Shield Plate	シールド板 (右)		05
110	VJ254100	Side Board	側板 (右)		04
120	VK350400	Bonding Tapping Screw	ボンドインクタッピングネジ	(3pcs)	01
130	EZ000460	Wheel Assembly	ホイール Ass'y		12
140	VK325400	Bonding Tapping Screw	ボンドインクタッピングネジ	(6pcs)	01
145	ED030066	Keyboard Assembly	鍵盤 Ass'y		52
150	EI340166	Bind Head Screw	バインド小ネジ	(4pcs)	01
160	VK350600	Bind Head Tapping Screw	バインドタッピングネジ	(4pcs)	01
170	ED030066	Angle Bracket-B, Earth	アースアングル (B)		06
180	EI040106	Bind Head Screw	バインド小ネジ	(9pcs)	01
190	VK350700	Bind Head Tapping Screw	バインドタッピングネジ	(8pcs)	01
200	ED030066	Angle Bracket-C, Earth	アースアングル (C)		05
210	EI040106	Bind Head Screw	バインド小ネジ	(6pcs)	01
220	XI246A00	Bind Head Tapping Screw	バインドタッピングネジ	(6pcs)	01
220	XI247A00	Power Transformer	電源トランス	J	12
220	XJ576A00	Power Transformer	電源トランス	U,C	12
230	EI040106	Power Transformer	電源トランス	H,D,A,B	12
235	CB069250	Bind Head Tapping Screw	バインドタッピングネジ	(2pcs)	01
240	--	Cord Clamper	束線止め		01
240	--	Power Supply Assembly	電源 Ass'y		
250	EI040106	Bind Head Tapping Screw	バインドタッピングネジ	(4pcs)	01
260	EI040106	Bind Head Tapping Screw	バインドタッピングネジ		
270	--	FDD Assembly	FDD Ass'y	C,A only	01
280	EI040106	Bind Head Tapping Screw	バインドタッピングネジ	(3pcs)	01
340	CB069250	Bind Head Tapping Screw	バインドタッピングネジ	(6pcs)	01
345	--	Cord Clamper	束線止め		
350	VK287400	Adhesive Tape	粘着テープ	(5pcs)	
360	EI040106	Circuit Board	DM1 シート		66
365	--	Bind Head Tapping Screw	バインドタッピングネジ	(6pcs)	01
370	VK287500	Isolation Sheet	絶縁シート		
375	CB040540	Circuit Board	DM2 シート		90
380	EI040106	Cord Clamper	S-72B L=50mm		01
390	VK351700	Bind Head Tapping Screw	バインドタッピングネジ	(6pcs)	01
390a	CB801270	Bottom Cover Assembly	底板 Ass'y		19
390b	ED340106	Foot	ゴム足	(4pcs)	01
400	VJ254100	Bind Head Screw	バインド小ネジ	(4pcs)	01
410	VJ254100	Bonding Tapping Screw	ボンドインクタッピングネジ	(24pcs)	01
415	VL413300	Bonding Tapping Screw	ボンドインクタッピングネジ		
416	ED340066	Name Plate	ネームプレート		11
420	VH811600	Bind Head Screw	バインド小ネジ	(6pcs)	01
430	CB825380	LCD Filter	保護板		06
440	--	Push Button	プッシュボタン	POWER	01
440	--	Caution Label	注意書		
455	--	Exciter Label	エキサイターラベル		
460	--	Name Label	銘板		
470	--	Earth Mark	アースマーク	A only	
480	--	Graphic Mark	グラフィックマーク	U only	
500	--	Head Protection Sheet	ダミーディスク		
	--	* ACCESSORIES	* 付属品		
	--	Plug Cover	プラグカバー		
	XI692A00	Floppy Disk	書込済み F D / B	J,A	
	XI693A00	Floppy Disk	書込済み F D / P	U,C	
	XI694A00	Floppy Disk	書込済み F D / G	H,D,B	
	--	Floppy Disk	書込済み F D	(Chick Korea)	

\*New Parts (新規部品)

ランク: Japan only

# **UPPER CASE ASSEMBLY (上ケースAss'y)**





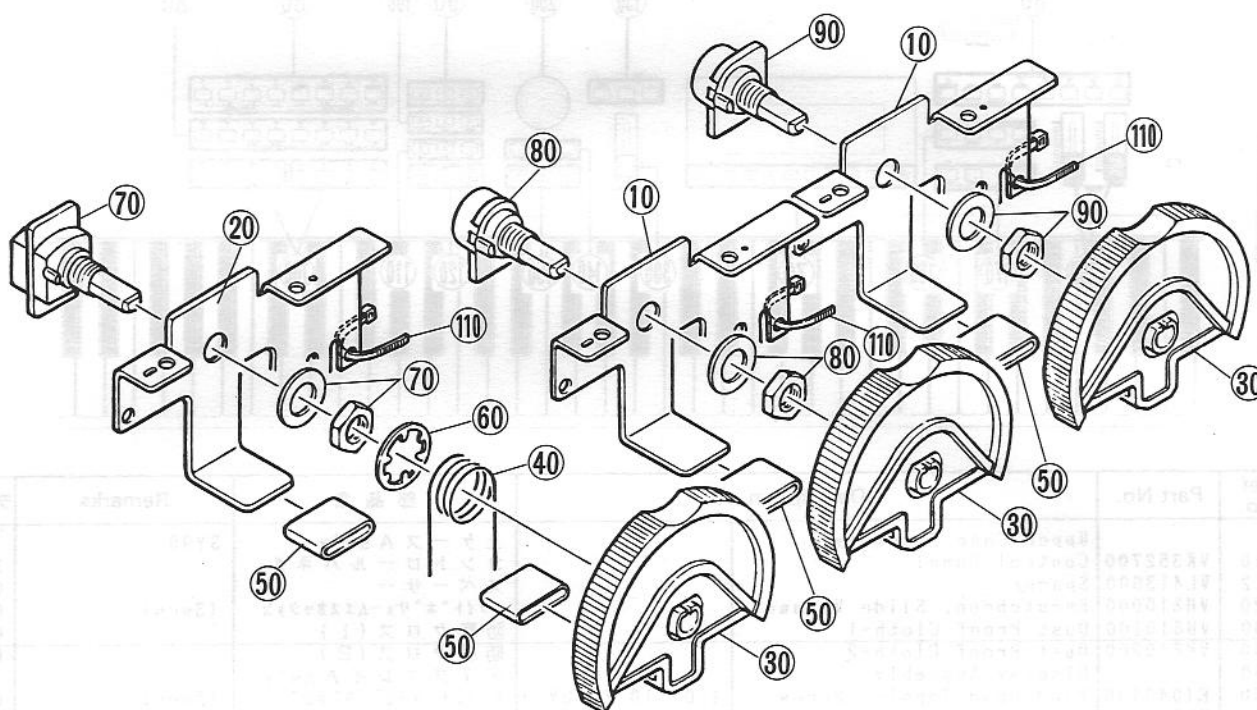
Ref No.	Part No.	Description	部品名	Remarks	ランク
10	VK352700	Upper Case Assembly	上ケース Ass'y	SY99	30
12	VL413600	Control Panel	コントロールパネル		05
20	VH810000	Spacer	スペーサー		02
30	VH810100	Escutcheon, Slide Volume	スライドボリュームエスケッション	(3pcs)	01
40	VH810200	Dust Proof Cloth-1	防塵クロス (1)		01
50	--	Dust Proof Cloth-2	防塵クロス (2)		01
60	E1040106	Display Assembly	ディスプレイ Ass'y	(2pcs)	01
70	VH811500	Bind Head Tapping Screw	ハインドタッピングネジ		03
80	VH810400	Function Key	ファンクションキー	(3pcs)	02
90	VI524400	Knob-A	ノブ A (8 連)		02
100	VI524500	Knob-B	ノブ B (3 連)	VWX, YZ', * &	02
110	VI524600	Knob-C	ノブ C (3 連)	MNO, PQR, STU	02
120	VI524700	Knob-D	ノブ D (3 連)	DEF, GHI, JKL	02
130	VI524800	Knob-E	ノブ E (3 連)	ABC, /., ., SPACE	02
140	VI524900	Knob-F	ノブ F (3 連)	<1, >, JUMP/MARK	01
150	VI534600	Knob-G	ノブ G (3 連)		03
160	VI537200	Knob-H	ノブ H (3 連)	-1/NO, +1/YES	03
170	VH810500	Knob-I	ノブ I (3 連)		01
180	VH810600	Knob-J	ノブ J (4 連)	(3pcs)	01
190	VH810700	Knob-K	ノブ K (飛3 連)		01
200	VK261900	Circuit Board	P N A B	P N A B シート	19
210	E1040106	Bind Head Tapping Screw	4.0 × 10 ZMC2Y	ハインドタッピングネジ	01
220	VI250800	Rotary Knob	ロータリーツマミ	Data entry Dial	01
230	VK261800	Circuit Board	PNC	PNC シート	23
240	E1040106	Bind Head Tapping Screw	4.0 × 10 ZMC2Y	ハインドタッピングネジ	01
250	--	Shield Sheet PNC	PNC シールドシート	(6pcs)	01
260	VL413100	Slot Unit Base	ユニットベース		09
270	VL413400	Rail-A	レール (A)	(5pcs)	03
280	VL413500	Rail-B	レール (B)	(5pcs)	03
290	VL413200	Slot Unit Cover	ユニットカバー		06
300	E1040106	Bind Head Tapping Screw	4.0 × 10 ZMC2Y	ハインドタッピングネジ	01
310	ED030066	Bind Head Screw	3.0 × 6 ZMC2Y	バインド小ネジ	01
320	ED340256	Bind Head Screw	4.0 × 25 FCM3BL	バインド小ネジ	01
330	CB817510	Cord Clamper	S-14B	束線止め	01
340	VK353100	Angle Bracket	Center	センターアングル	10
350	E1040106	Bind Head Tapping Screw	4.0 × 10 ZMC2Y	ハインドタッピングネジ	01
360	--	Shield Sheet DM1	DM1 シールドシート		
370	--	Shield Sheet DM2	DM2 シールドシート		
380	--	Shield Sheet MK	MK シールドシート		
390	E1040106	Bind Head Tapping Screw	4.0 × 10 ZMC2Y	ハインドタッピングネジ	01
400	VK666500	Circuit Board	CN	CN シート	(16pcs)
410	ED030066	Bind Head Screw	3.0 × 6 ZMC2Y	バインド小ネジ	01
420	VH812800	Card Guide	カードガイド	(6pcs)	06
430	E1040106	Bind Head Tapping Screw	4.0 × 10 ZMC2Y	ハインドタッピングネジ	01
440	E1040106	Bind Head Tapping Screw	4.0 × 10 ZMC2Y	ハインドタッピングネジ	01
450	VJ875400	Circuit Board	JK	JK シート	(3pcs)
460a	NX809690	Circuit Board	JK (JK)	JK (JK) シート	
460b	NX809700	Circuit Board	JK (JKB)	JK (JKB) シート	
460c	NX809710	Circuit Board	JK (CARD)	JK (CARD) シート	
470	VJ254100	Bonding Tapping Screw	4.0 × 10 MFZN2BL	ボンディングタッピングネジ	(10pcs)
480	ED340106	Bind Head Screw	4.0 × 10 FCM3BL	バインド小ネジ	(1pcs)
490	VB774000	Knob	ツマミ	VOL, D. ENTRY (3pc)	01
500	--	Adhesive Tape	粘着テープ	(3pcs)	01
510	CB069250	Cord Clamper	BK-1	束線止め	(3pcs)

\*New Parts (新規部品)

ランク: Japan only



# WHEEL ASSEMBLY (ホイールAss'y)

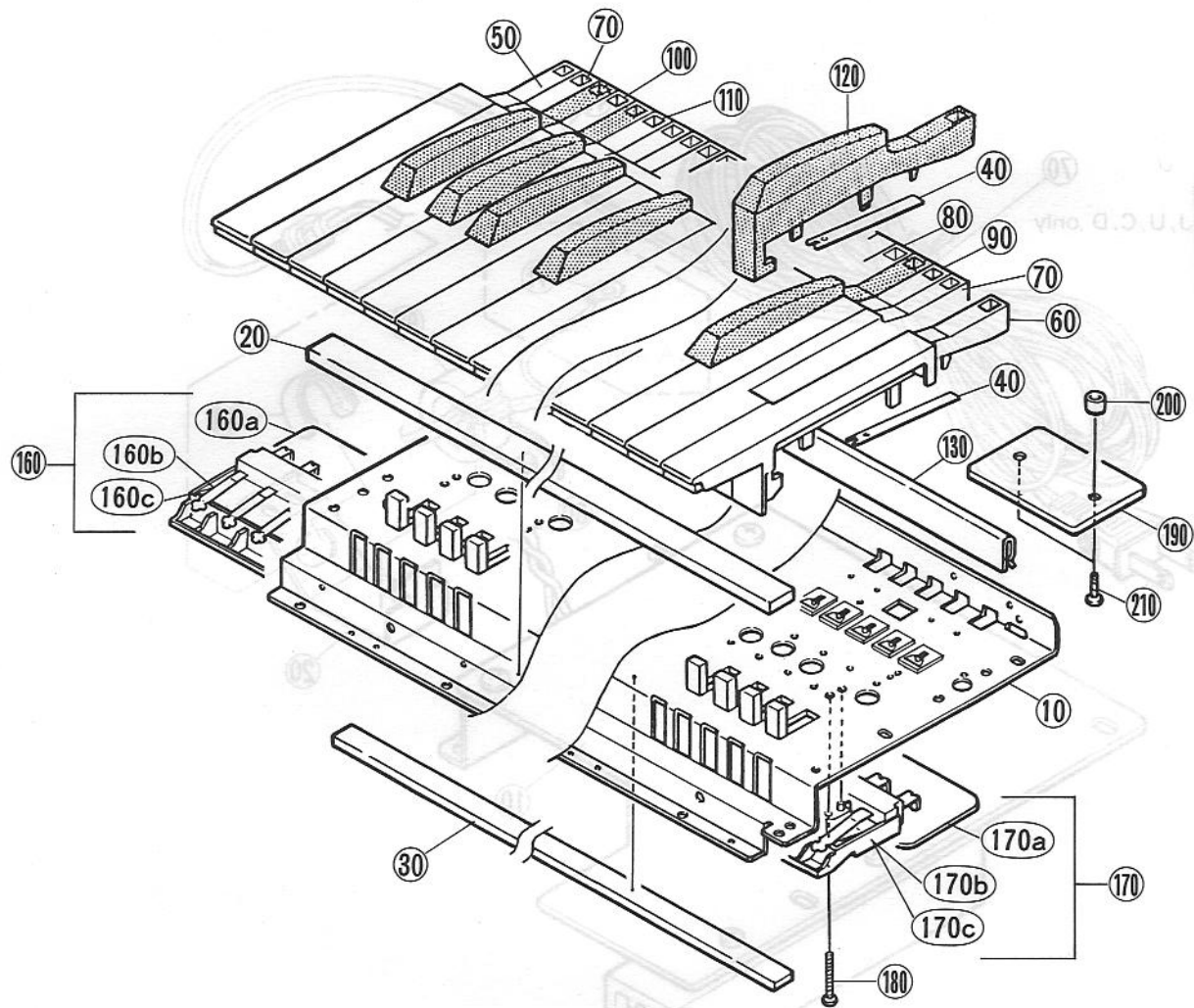


Ref. No.	Part No.	Description	部品名	Remarks	ランク
		Wheel Assembly	ホイール Ass'y	SY99	
10	VF536800	Frame	フレーム	MOD. 1,2 (2pcs)	01
20	VJ187600	Frame-A	フレーム (A)	PITCH BEND	02
30	VF537400	Wheel	ホイール	(3pcs)	02
40	VC792800	Spring	リターン スプリング	PITCH BEND	01
50	CB819020	Wheel Tube	ホイールチューブ	(4pcs)	02
60	EW600110	Wheel Ring	C S 形止め輪	PITCH BEND	01
70	VK588200	Variable Resistor	ロータリーボリューム	PITCH BEND	03
80	HS412160	Variable Resistor	ロータリーボリューム	MODULATION 1	03
90	VI666700	Variable Resistor	ロータリーボリューム	MODULATION 2	03
110	CB069250	Cord Clamper	束線止め	(3pcs)	01

\*New Parts (新規部品)

ランク : Japan only

# **KEYBOARD ASSEMBLY (鍵盤Ass'y)**

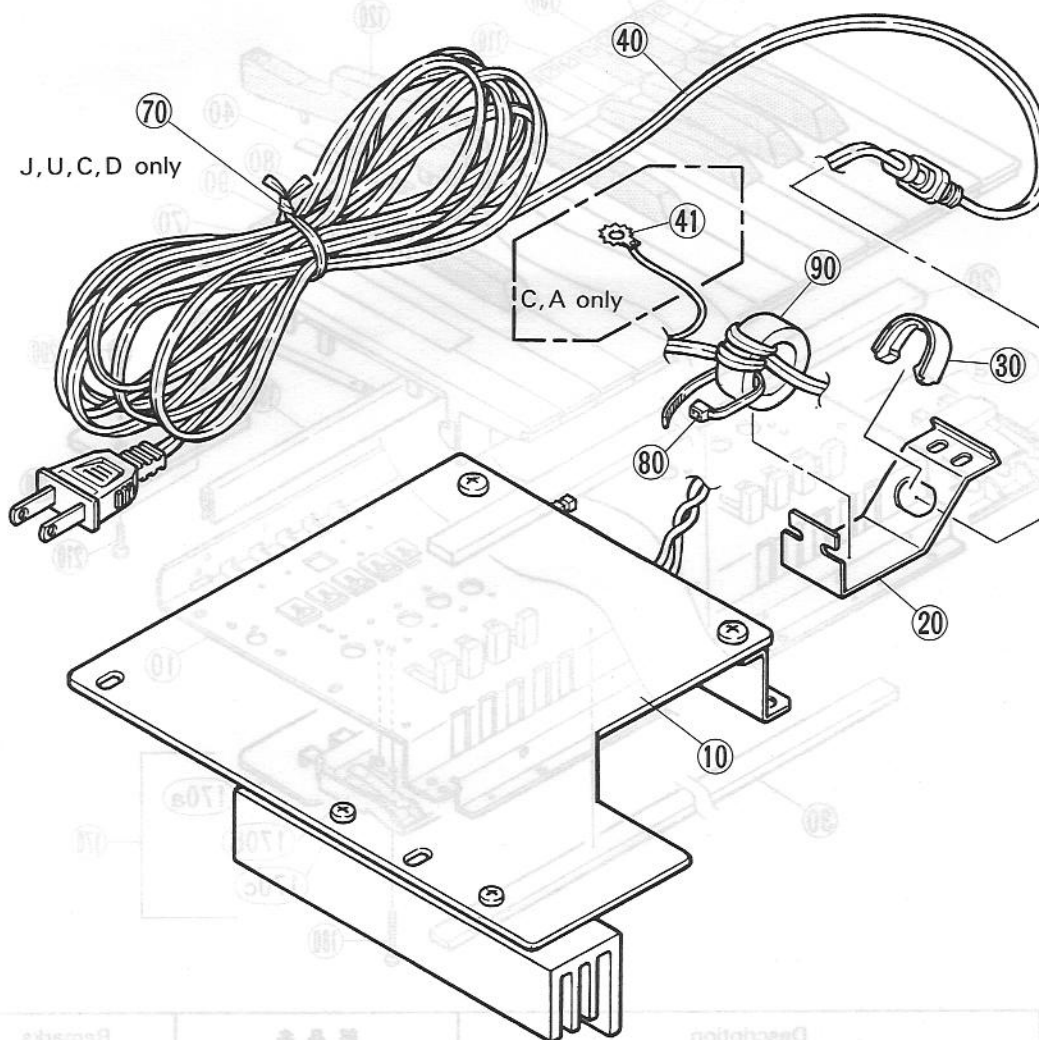


Ref. No.	Part No.	Description		部 品 名	Remarks	ランク
10	VK325400	Keyboard Assembly	FS E76	鍵盤 Ass'y	SY99	52
20	VK735000	MK Frame	FS E76.	MK フレーム		11
30	VK659200	PC Sensor		PC センサー		04
40	AA055430	Felt	WH 1027×6×3	フェルト (白)		02
50	NB826010	Key Spring		鍵バネ	(76pcs)	04
60	NB826020	White Key Assembly	E'	白鍵 Ass'y		04
70	NB107540	White Key Assembly	G'	白鍵 Ass'y	(13pcs)	03
80	NB107550	White Key Assembly	C, F	白鍵 Ass'y	(6pcs)	03
90	NB107560	White Key Assembly	D	白鍵 Ass'y	(12pcs)	03
100	NB107570	White Key Assembly	B, E	白鍵 Ass'y	(6pcs)	03
110	NB107580	White Key Assembly	G	白鍵 Ass'y	(6pcs)	03
120	NB107600	Black Key Assembly	A	黒鍵 Ass'y	(31pcs)	03
130	VK325600	Stopper	FS E76	ストッパー		04
160	NB825940	Key Switch Unit	FS E76	MK スイッチユニット		17
160a	NA810850	Circuit Board	MK1	MK シート		07
160b	NB107130	Key Switch Assembly	9I FS	スイッチ Ass'y		08
160c	NB107120	Key Switch Assembly	12Q FS	スイッチ Ass'y	(2pcs)	08
170	NB825950	Key Switch Unit	FS E76	MK スイッチユニット		19
170a	NA810860	Circuit Board	MK2	MK シート		08
170b	NB107120	Key Switch Assembly	12Q FS	スイッチ Ass'y	(3pcs)	08
170c	NB107150	Key Switch Assembly	7G FS	スイッチ Ass'y		08
180	ED330166	Bind Head Screw	3.0×16 FCN3BL	スライド小ネジ	(20pcs)	01
190	VK263600	Circuit Board	PC	PC シート		08
200	VA032600	Spacer		スペーサー	(2pcs)	01
210	ED030126	Bind Head Screw	3.0×12 ZMC2Y	バインド小ネジ	(2pcs)	01

\*New Parts (新規部品)

ランク : Japan only

# POWER SUPPLY ASSEMBLY (電源Ass'y)

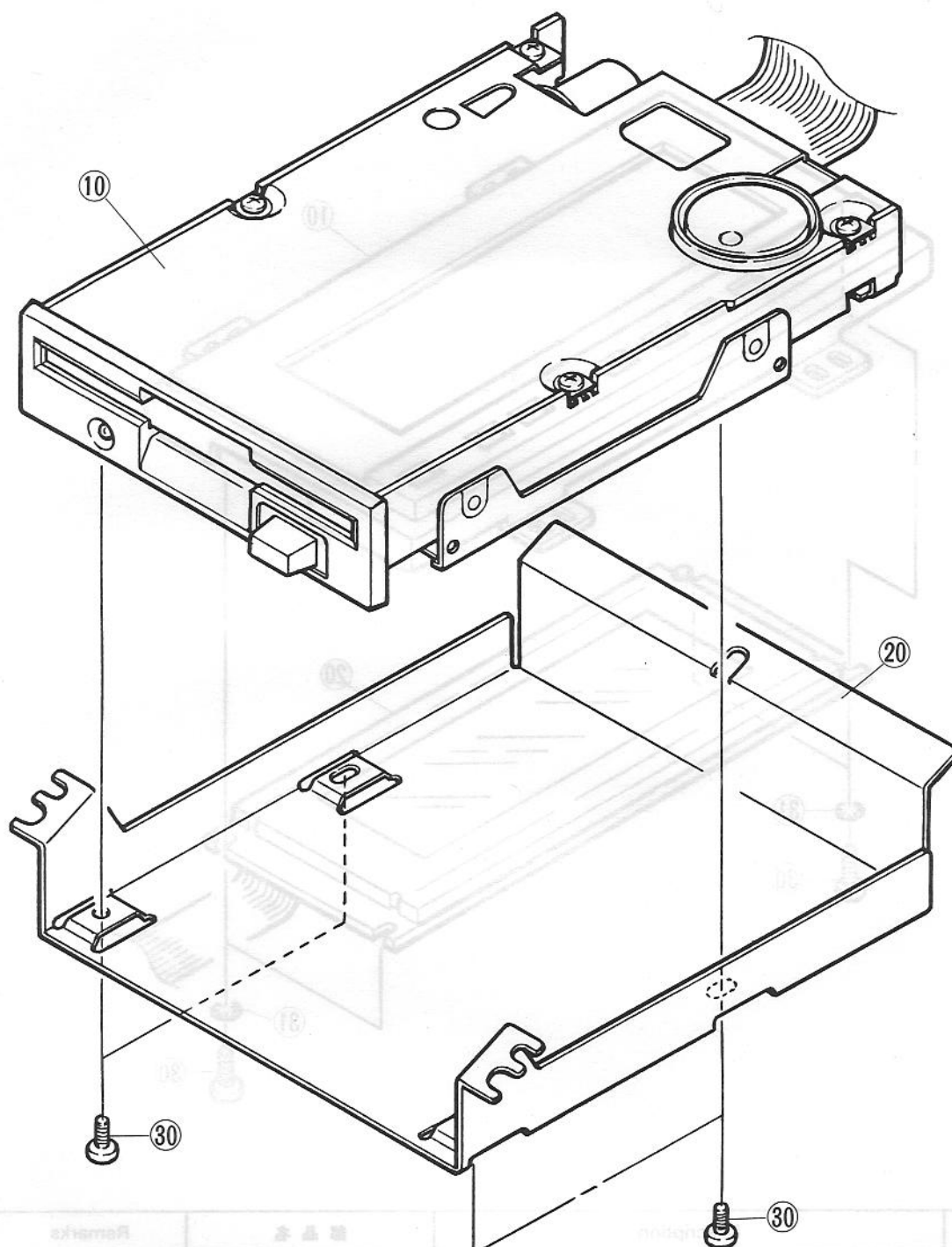


Ref. No.	Part No.	Description	部品名	Remarks	ランク
10	VJ800200	Power Supply Assembly	電源 Ass'y	SY99	19
10	VJ800300	Circuit Board	PS シート	J	20
10	VJ800400	Circuit Board	PS シート	U	20
10	VJ800500	Circuit Board	PS シート	C	20
20	VH812600	AC Panel	AC パネル	H, D, A, B	02
20	VI319500	AC Panel	AC パネル	J	02
20	VI319600	AC Panel	AC パネル	U	02
20	VI319700	AC Panel	AC パネル	C	02
30	CB811230	Cord Strain Relief	コードストッパー	H, D, A, B	02
30	CB806850	Cord Strain Relief	コードストッパー	U	02
30	CB072750	Cord Strain Relief	コードストッパー	C	01
30	CB032840	Cord Strain Relief	コードストッパー	H, D, B	01
40	VD279200	AC Cord	電源コード	A	04
40	VD279400	AC Cord	電源コード	J	06
40	VD279500	AC Cord	電源コード	U	07
40	VD280400	AC Cord	電源コード	C	06
40	VD279700	AC Cord	電源コード	H, D	06
40	VH890400	AC Cord	電源コード	A	06
41	LA003690	Lug Terminal	端子	B	08
70	--	Cord Clamper	ビニタイ	C, A only	01
80	CB069250	Cord Clamper	束止め	J, U, C, A only	01
90	VC362700	Ferrite Core	フェライトコア		04

\*New Parts (新規部品)

ランク : Japan only

# FDD ASSEMBLY (FDD Ass'y)



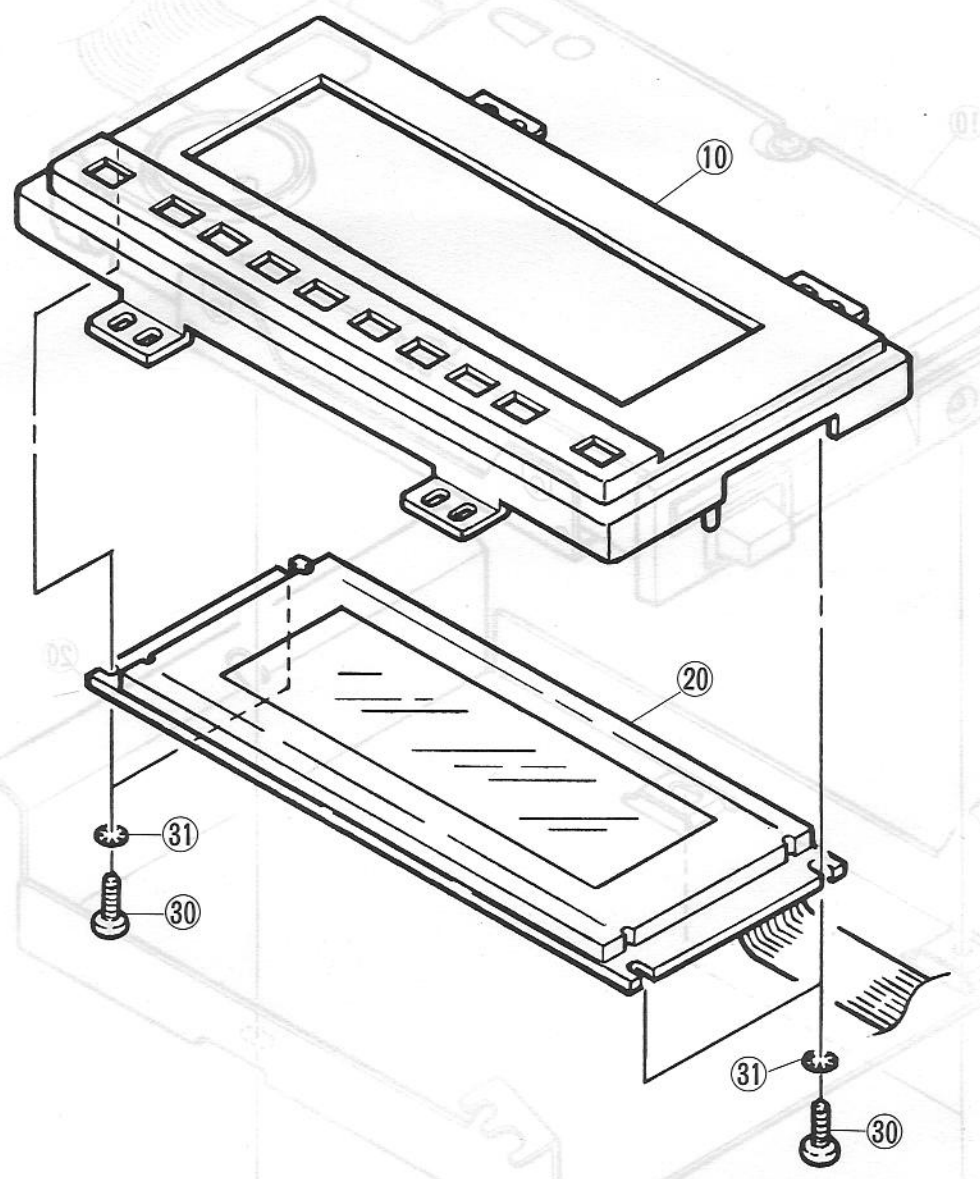
Ref. No.	Part No.	Description	部品名	Remarks	ランク
10	VK423800	FDD Assembly	FDD Ass'y	SY99	24
20	VH813000	Floppy Disk Driver	フロッピーディスクドライブ	3.5"	04
30	ED330066	Angle Bracket, FDD	FDD 金具	(4pcs)	01
		Bind Head Screw	バインド小ネジ		

\*New Parts (新規部品)

ランク : Japan only



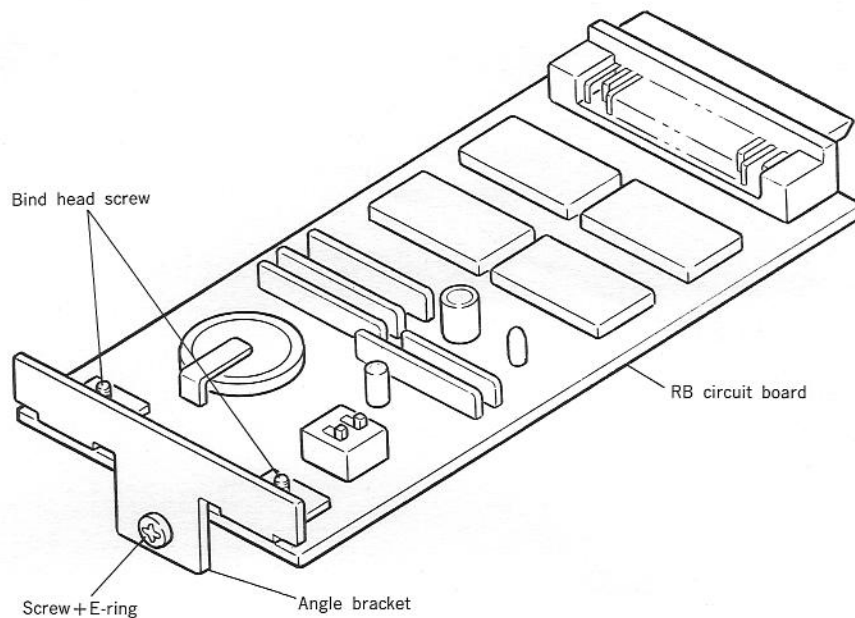
■ DISPLAY ASSEMBLY (ディスプレイ Ass'y)



Ref. No.	Part No.	Description		部 品 名	Remarks	ランク
10	VH811400	Display Assembly Escutcheon, LCD		ディスプレイ Ass'y LCD エスカッション	SY99	05
20	VK372800	LCD Assembly		L C D   A s s ' y		
30	E1330086	Bind Head Tapping Screw	3.0×8 FCM3BL	ハインドヘッドタッピングネジ	(4pcs)	01
31	EV413036	Toothed Lock Washer	A φ 3.0 FCM3BL	歯付座金内歯形	(4pcs)	01



# EXPANSION MEMORY BOARD (SY拡張メモリーボード) SYEMB05



Ref. No.	Part No.	Description		部品名	Remarks	ランク
	--	<RAM Board>	SYEMB05	<SY拡張メモリーボード>		
	VL413800	Circuit Board	RB	R B シート		09
	ED030066	Angle Bracket RB		ボードアングル		01
	VL413700	Bind Head Screw	3.0×6 ZMC2Y	バインド小ネジ	(2pcs)	04
	EV501256	Screw	SWCH12A	ボードネジ	(1pc.)	01
		E-Ring	φ 2.5 FNM3-3G	E 形止め輪	(1pc.)	01
	--	Circuit Board	RB	R B シート		
	XI686A00	IC	MG2021FP	I C	SYST.RESET (1pc)	04
	--	IC	TC74HC08AF-TP1	I C	AND (1pc.)	
	--	IC	HM628128LFP-10	I C	SRAM 1M (4pcs)	
	VB797600	Diode	RLS-73 0.1A	ダイオード	(1pc.)	01
	VE331300	Resistor Array	RGLD8X104J	抵抗アレイ	100K×8 (4pcs)	01
	VL972100	Resistor Array	EXB-F7E104J5	抵抗アレイ	100K×6 (1pc.)	01
	RD256470	Chip Resistor	4.7KΩ 0.1W J	チップ抵抗	(1pc.)	01
	RD257100	Chip Resistor	10KΩ 0.1W J	チップ抵抗	(2pcs)	01
	RD257470	Chip Resistor	47KΩ 0.1W J	チップ抵抗	(1pc.)	01
	--	Chip Monolithic Cera. Cap.	F 0.1μ 25V Z	チップ積層セラコン	(7pcs)	
	--	Slide Switch	KSD02	スライドスイッチ	(1pc.)	
	VL347500	Connector FX2	FX2-52S-1.27DSI	F X 2 コネクター	52P SE (1pc.)	04
	VE338400	Lithium Battery	SONY/CR2032 3V	リチウム電池	(1pc.)	03

\*New Parts (新規部品)

ランク: Japan only

